**Laboratory 6  
Instrumentation amplifier**Today’s lab is a mini-quiz. You are allowed to discuss with your group for the design & analysis of   
Parts A to C – get your answers checked in sequence. Circuit building & testing happens in Part D.

**A**: /7 **B**: /3 **C**: /6 **D:** /4 **Tot:** /20

The term ‘instrumentation amplifier’ is generally used to denote an amplifier that has the following properties:

1. High gain
2. Accepts a differential input
3. Has very high input impedance
4. Produces a single ended output with reference to a user supplied Vref
5. Has very small output impedance
6. Has very high CMRR

In this assignment we will build up an instrumentation amplifier in steps to satisfy each of the above criteria

Recall the diagram of a measurement system shown in Fig 1, which we discussed in the introductory lecture:

Fig 1: Typical measurement system with an instrumentation amplifier

Physical System



+VA

-VA

*iA*

*iA*

Amplifier

+VR

*iR*



*iR*

Readout  
(DSO)

Signal *Ss* ±***δ***

Signal ***Δ***

**Introduction – definition of CMRR**

The steady state currents consumed by the three components: Source *is* Amplifier *iA* Readout *iR* are usually very different. Hence the steady state signals generated by the three devices *SS SA SR* will also be different. These can be voltage or current signals.

The source is a transducer that converts a physical effect (eg: light shining on a photo-diode, pressure measured by a piezo sensor etc…) into a small electrical signal *δ* centered around the steady-state value *SS.* For a *voltage* source: *SS* is typically set to (*VS /2*) so as to maximize the ‘dynamic’ range: *Ss* ± *δ* **=** *Vs/2* ± *δ* is allowed to swing the through the full range between *VS* and 0.

This places a restriction on the design of the amplifier with (large) gain *G*: The amplifier’s output *SA = G\*(Ss* ± *δ)* would normally be so large as to always keep *SA* saturated.   
Therefore the amplifier, which we now call an instrumentation amplifier, must operate such that the steady-state source signal *SS* is rejected and only the dynamic part ± *δ* is amplified: *SA =* ± *Δ = G\*(*± *δ)*This principle is called Common Mode Rejection, and it is quantified by the Common Mode Rejection Ratio (CMRR)

Mathematical definition of CMRR: Consider a two-terminal device which produces voltages *V1 V2 at its terminals. The signal input to the amplifier is* *Vin = (V1  - V2).*  An amplifier with differential signal gain *AD provides Vout = AD∙Vin*  The common mode signal is defined as *Vcm=(V1 + V2­)/2* and the common-mode gain is *ACM = Vout/Vcm.* The CMRR is defined by the following formula. You want to have it as large as possible. The ‘bare’ opamp has an intrinsic CMRR (look this up in the datasheet). A feedback circuit to stabilize the gain will almost always reduce the CMRR.

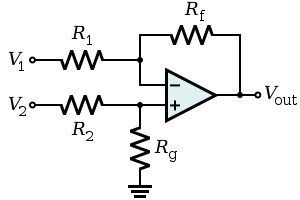
Intelligent circuit design is required to keep the CMRR as high as *practically* possible.

**Part A: Difference amplifier**

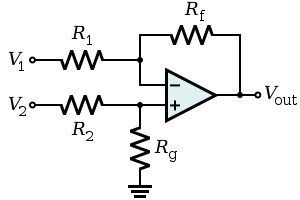
Consider the simple difference amplifier circuit in Fig 2(a). It has the two voltages *v1 v2* as input. To begin with let us consider *v1 & v2* as two *independent voltages –* we are interested in what happens to the *difference (v1 – v2)*

Fig 2(a): Difference amplifier – all resistors are of equal value R

Fig 2(b): Difference amplifier – space for analysis



Vref



0

**Q1:** What is the input impedance seen by *v1*in Fig 2(a) ? Ans: *R*

/1

/1

/1

/1

/1

/1

/1

**Q2:** What is the input impedance seen by *v2*in Fig 2(a) ? Ans: 2*R*

**Q3:** Use KVL to determine the voltages at each node of the circuit in Fig 2(a) – mark your answers in the circuit of Fig 2(b)  
*Hint: Since the opamp draws no current, the voltages at its (+) and (-) terminal are always equal [Golden Rule 1 of opamp design!]*

**Q4:** Using the answers to Q3, What is the relation of *vout to (v1 – v2)* ?  
*Hint: As discussed in the lecture, you can use superposition – set v1 and v2 to zero one at a time and determine vout*

Ans: *vout = (v1 – v2)*

**Q5:** Suppose you have a common mode voltage *vcm=(v1 + v2)/2* always­ present, what is the relation of *vout to vcm* ?

Ans: *vout = 0*

**Q6:** In the above calculations, *vout* is referenced to the 0Vshown in Fig 2(a). Suppose 0Vis replaced by an arbitrary user defined voltage *Vref* in the box shown in Fig 2(b). How does your answer to Q4 change? *Vout = function(v1-v2)*

Ans: *stays the same: vout = v1 – v2*  ; *vout* is now referred to *Vref not 0V*

**Q7:** Basedon your answers to the above questions, list the criteria of the instrumentation amplifier design that a difference amplifer *does* *not* satisfy

Ans:  *Low and asymmetrical input impedance.*

**Part B: Evolution of the difference amplifier design**

Let us work on improving the difference amplifier of Part A by fixing its problems one at a time:

**B1:** The most severe problem is obviously that the input impedance presented to *Vin* is small

Add requisite blocks to the difference amplifier so that the input terminals *v1* and *v2* look into large (equal) impedances. Draw your modified block diagram here.

Solution:

Obvious thing is to add unity gain buffers in line between *v1* and *v2* each to the inputs of the difference amplifer

/0.5

/0.5

/2

**B2:** The second obvious problem is the high gain requirement for the instrumentation amplifier, which we have not gotten out of the difference amplifier yet.

Investigate ways of providing large gain to the *differential* signal *vd =* (*v1 – v2)*  
Draw your possible design of a high gain, high input impedance differential amplifier here:

Students may want to

1. Add finite gain to the unity gain blocks. This has the problem that gain of each is set by a separate set of *Rf/R0* resistors. So depending on slight variations in resistor values, *v1* and *v2* will have unequal gain in their paths.
2. Add finite gain to the final stage difference amplifier.

(1) is preferable, but both the above lead to high *ACM* as calculated below.

**Important:** For whatever design you make here, calculate *both* the differential gain *AD* and the common-mode gain *ACM* of your design. Recall that our final objective is to make *AD* very high while keeping *ACM* as low as possible for high CMRR.

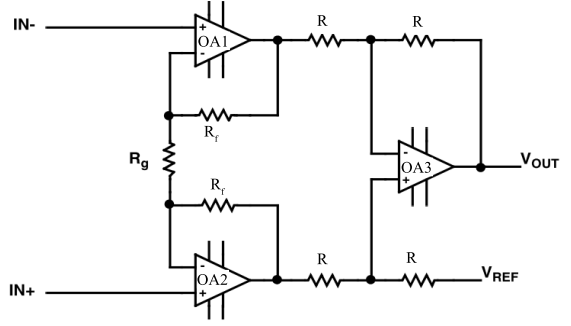
Instructor’s note: typically this assignment is done just before midsem. Parts A+B can be   
completed in one afternoon. Students may need one more session to read up references and  
 complete Part C. Try to arrange an extra afternoon in the same week for students to complete the instrumentation amplifier design in Part C in the same week (else they will have forgotten Parts A+B by the time they come back after midsem)

**Part C1: Final design of Instrumentation amplifier**

By now, you should have solved most of the problems of the simple difference amplifier to arrive at a *nearly* good instrumentation amplifier. **Except** we still need to:

1. Minimize the common mode gain *Acm* to get a high CMRR
2. Reduce dependence on values of discrete passive parts like resistors. Ideally, the entire circuit should use just one value of the resistor R, and the gain must be set by one gain setting resistor *Rg*

Make the requisite improvements to design of Part C to arrive at the final design of a 3 opamp instrumentation amplifier which satisfies all the 7 criteria listed on page 1.



Solution:

/1: *AD* /2.5:*Acm*

/4

/2.5

Resistor matching not critical – need six matching *R (if we use Rf = R)*, Gain is set by *Rg***Part C2: The CMRR – is it good?**

Calculate the differential and common mode gains *AD* and *ACM*  of your design  
*Hint: Use Golden Rule 1 and superposition for AD. Determine the quantity and directions of current flow with v1=v2 for Acm*

*AD=R/Rg* For *v1=v2 no current flows through Rg so each of OA1 and OA2effectively reduce to unity gain and Acm=1*

**Part D: Test of Instrumentation amplifier**Build and demonstrate the operation of your 3 opamp instrumentation amplifier designed in Part C. You may set G=10. Use a differential sine wave signal of small magnitude as *Vin* Demonstrate the high CMRR of your design by applying an offset to *Vin* and checking if the offset is rejected by the circuit.

Note that the three opamp instrumentation amplifier is often available as a pre-packaged IC (for example AD524). All the resistors are precision matched within the IC – only 2 external pins are provided to connect the gain setting resistor.