Name: *Roll Number:*

A: /5	B: /4	C: /6	Tot: /15

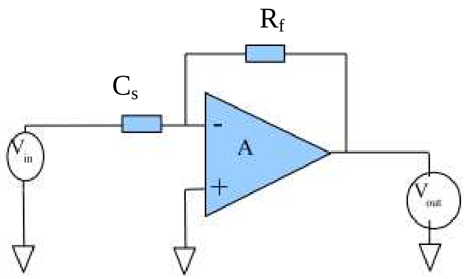
Laboratory 8

Relaxation Oscillators

This lab consists of three modules. We will see how parasitic effects can occasionally be used to a designer's advantage

Part A: Capacitor connected at Input

Fig 1: C_s at source



Consider the circuit of Fig 1. Notice the difference from standard inverting feedback amplifier: the *source* resistor has been replaced by a capacitor C_s.

Q1: Calculate the *time-domain* response of V_{out} to V_{in} as in Part A. The time-domain response requires you to apply the golden rules of opamp design *and* the current-voltage relationship for a capacitor $I = C\ {}^{dV}/_{dt}$ followed by some algebra.

Current at (-) input : $V_o/R + C\ dV_{in}/dt = 0$ so $V_o = -RCdV_{in}/dt$ → Differentiator (with – sign)

/2

Q2: Choose suitable values of the passive components R_s, C_f such that the time constant of your design is 1 ms.

/1

Q3: Build the circuit of Fig 2 and drive it with a *square* V_{in} of amplitude 2V peak-to-peak.
Note that C_s is in the signal path, so the type of capacitor used is important. Choose wisely!
Draw a diagram of your observations here and verify that your calculations of Q1 above are correct.

Square differentiate → flat 0 *except* +/- delta functions at edges
Delta function → opamp output saturates and rings after it comes out of saturation.
Can fix this by adding *R_f/2 in series* with C_s to set a very low gain.

/2

Part B: Comparator

Recall the simple comparator (with hysteresis) circuit using positive feedback we studied earlier in Lab 2. The function of a comparator is to feedback a fraction of V_{out} to the **(+)** input so that when V_{in} exceeds a threshold set by the feedback fraction R_f^+/R^+, the output switches to $-V_{sat}$ and when V_{in} falls below threshold, output switches to $+V_{sat}$

Use your memory/logic and draw the diagram of a simple comparator circuit here:

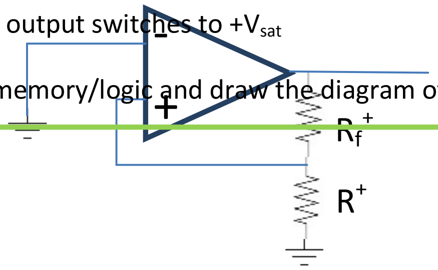


Fig 2: Simple comparator with positive feedback. Set the reference voltage for comparison to $V_{sat} *(R^+/R_f^+ + R^+)$

/1

/0.5

<u>Q1:</u> For V_{in}= 0, <u>*predict*</u> the values of V_{out} in your circuit:

a) What is V_{out} at t=0 <u>immediately</u> when the circuit is turned on?

0V

/0.5

b) For an *ideal* power supply that turns on $+/-V_{cc}$ as a step function, what is V_{out} in the very short time ~ microseconds after the circuit is turned on?

Rises to + or - V_{sat} limited by the slew rate ~ 0.1/µs : so it will take ~ 10 µs to reach V_{sat}

/0.5

c) What is V_{out} in steady state after the circuit has been on for a few seconds:

$+/- V_{sat}$

/0.5

d) What determines the steady state value of V_{out} in question c) ?

Sign of input offset voltage V_{os}

<u>Q2:</u> Connect up the circuit you have designed in Fig 2 and *demonstrate* the validity of your predictions Use this space to record your DSO observations of V_{out} in detail.

Note that V_{in} = *0* for a), b), c)

Your observations for (b) may differ from prediction because the power supply is *not* ideal. Observe the voltage $+/-V_{cc}$ supplied by the power supply to the circuit at t=0 on the DSO to validate your prediction.

Part C: Relaxation oscillator

Use your observations and conclusions from Parts A and B to make a circuit ***with one opamp*** that demonstrates the following behavior:

1. It's V_{out} oscillates between two fixed values (for example $+V_{sat}$ and $-V_{sat}$)
2. It has no external V_{in} applied
3. The oscillation time period is 1 ms

Hint: You will need to combine the concepts of Parts A and B

Draw your circuit design here. Calculate and mark the value of the components required.

Comparator with differentiator in negative feedback loop
Relies on delta function created by 0 to $+V_{sat}$ switching to force output to switch to $-V_{sat}$ and vice-versa

/2.5

/3.5

This type of oscillator is called a 'Relaxation Oscillator'. Build your circuit and demonstrate its operation

/2