

Lecture 6

Review of Instrumentation Amp

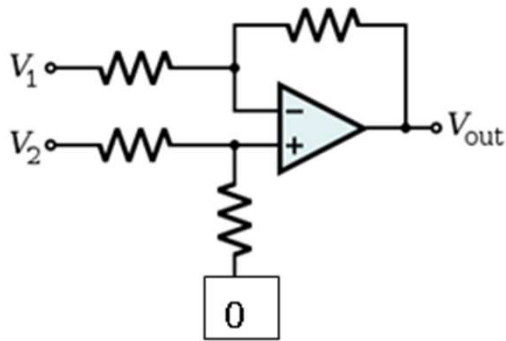
Impedance matching – power transfer

Reference:

“bible” of RF circuit design:

Thomas H. Lee “The design of CMOS Radio-Frequency Integrated Circuits”

Review of Lab 5 – Instrumentation Amplifier



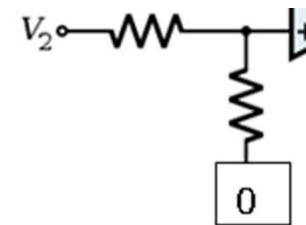
Impedance looking into V_1

Set V_2 to zero

$$\rightarrow v_+ = 0$$

$$\rightarrow v_- = v_+ = 0$$

$\rightarrow V_1$ sees resistance \mathbf{R} to ground



Impedance looking into V_2

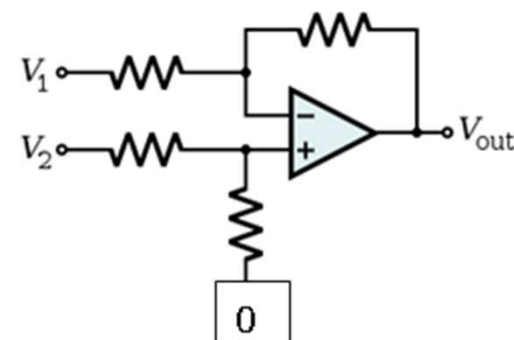
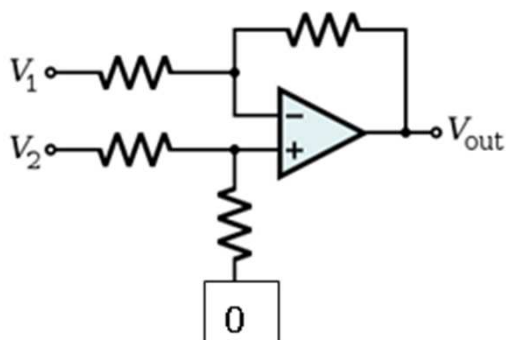
Set V_1 to zero

\rightarrow No current into v_+

\rightarrow Can 'ignore' the bulk of the circuit

$\rightarrow V_2$ sees resistance $\mathbf{2R}$ to ground

Response of difference amplifier



Difference Response:

$$V_1 \neq 0, V_2 = 0$$

$$v_- = (V_{out} - V_1)/2 \quad v_+ = 0 \rightarrow v_- = 0 \rightarrow V_{out} = V_1$$

$$V_2 \neq 0, V_1 = 0$$

$$v_+ = V_2/2; \quad i_+ = V_2/R; \quad i_- = V_{out}/R$$

$$i_+ + i_- = 0 \rightarrow (V_{out} + V_2)/R = 0 \rightarrow V_{out} = -V_2$$

Superposition: $V_{out} = V_1 - V_2$

Common mode response

$$V_1 = V_2 = V_{cm}$$

$$v_+ = V_{cm}/2 \quad v_- = V_{cm}/2 \text{ (by golden rule)}$$

$$v_- = (V_{out} + V_{cm})/2 \text{ (current sum at } v_- \text{ terminal)}$$

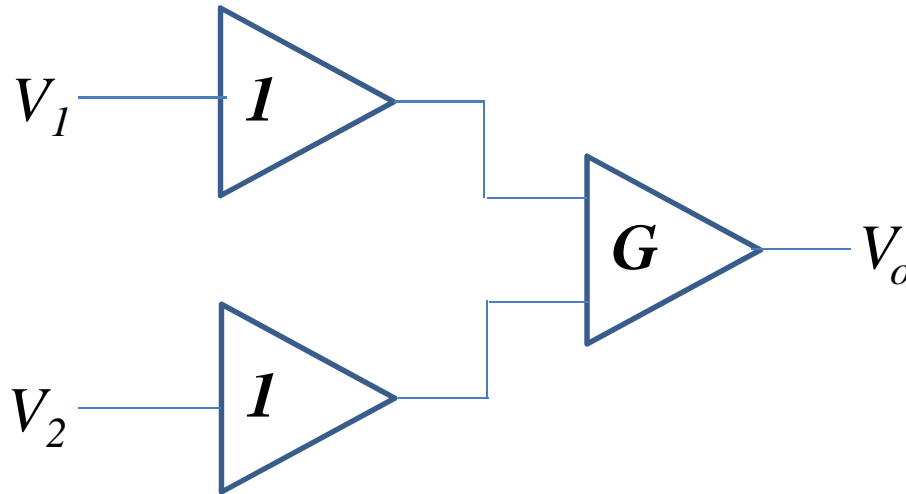
$$V_{out} = 0$$

Assuming ideal case 4 R's equal

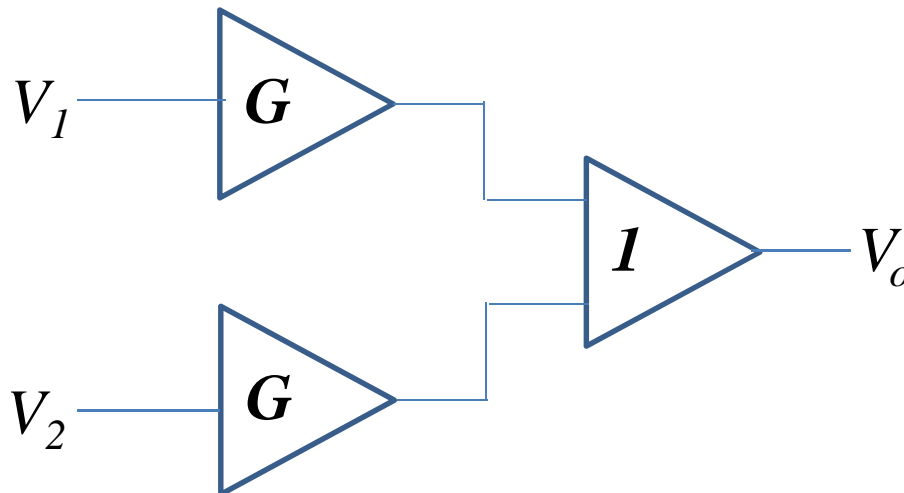
In practice:

$$V_o = V_{cm} \left(\frac{R_4}{R_3 + R_4} \right) \left(1 - \frac{R_2 R_3}{R_1 R_4} \right)$$

It is best to put the gain stage as close to the input signal as possible



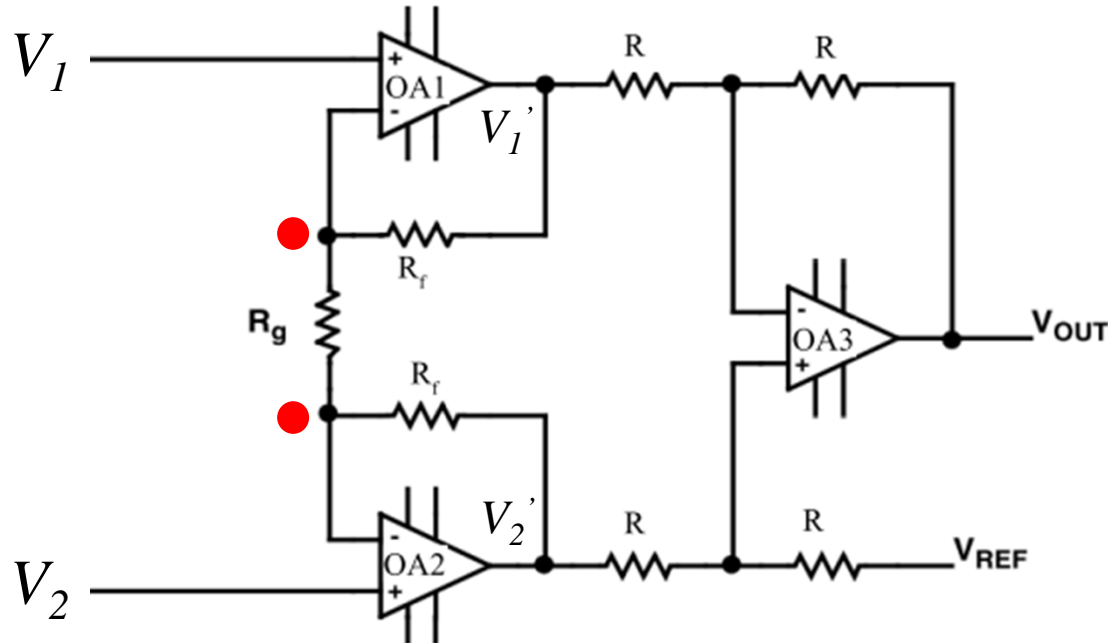
- ☺ Inputs see high impedance
- ☹ Difference amplifier gain G no longer has $A_{cm} = 0$
- ☹ S/N is worsened by noise of unity gain buffer



- ☺ Inputs see high impedance
- ☺ Difference amplifier has $A_{cm} = 0$
- ☹ Need precise component matching to get equal G for V_1 and V_2

Kill two stones with one bird

Reduce component count, Increase CMRR



*Differential Gain is set by R/R_g
(Easy to calculate by superposition)*

Common mode: $V_1 = V_2$

v_- of OA1 and OA2 are equal (two red dots)

→ No current flows through R_g

$V_1 \rightarrow V_1'$ and $V_2 \rightarrow V_2'$

- ☺ Inputs see high impedance
- ☺ All resistors equal except R_g
- ☺ V_o referred to V_{ref}
- ☺ $A_{cm} \sim 0$ within tolerance of $6R, R_g$