**Laboratory Assignment 6 : Common Emitter Amplifier**

Marks **A: /5** **B1: /2 B2: /3** **B3:** /**2 B4: /3**  **Tot= /15**

**Goal: [Complete Part A1 individually first before continuing further]**

In Lab 5, you set up a BJT in common-emitter (CE) mode and found the associated passive components to be added to the circuit mostly by trial/error/consultation. Today we will go through a systematic procedure of how to 'bias' the transistor so that it behaves linearly as an amplifier.

Fig 1 shows a CE amplifier with appropriate 'resistor-bias' circuit. The 7-step procedure to determine the component values is detailed below. The exercises begin on Page 2.

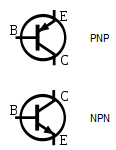


Fig 1: CE amplifier without feedback

C1

Function

Generator

**+**

**-**

Vload

R1

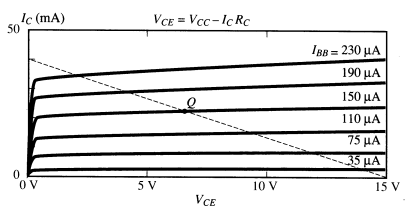
RC

R2

RE

C2

Vcc



*Large Vout*

*Small Vin*

BJT CE Characteristics

from Lab 4  
dashed line with descending slope indicates the   
DC ‘load’ line.   
Vload = VCC – ICERC

re

10 V

**The Design Process is split in two independent parts: First we do DC design to bias the BJT in Active mode, then the AC design is done to make the amplifier amplify AC signals  
Steps 1 – 4 : DC Design:**

Capacitors block DC signals, so for this part, ignore all the capacitors. Capacitors are treated as   
open-circuit in DC analysis (i.e. no connection from one two terminals of the capacitor)

***Step 1: Choose the quiet operating point Q for IC: ICQ***

*ICQ* is given as an input to the design. The designer chooses *ICQ* based on:

a) desired power dissipation in the circuit – the amplifier will dissipate power *ICQRC* at idle.

b) load – how much current does the load connected to *Vload* need?

***Step 2: Choose RC***

We need to center *Vload* at the halfway point between *VCC* and ground. With *IC* from Step 1, this determines *Rc*

***Step 3: Choose RE***

Place *VE* at *~ 1V* for thermal stability of the transistor. Assume *IC=IE*  This determines *RE*

***Step 4: Determine R1 andR2***

For transistor to be in active mode, *VBE* must be at least  *0.6V.*  Here we have already set *VE* at *1V,* so *VB* must be *1.6V.* Assuming negligible current flow into base at DC determines the ratio *R1/R2* as a voltage divider between *VCC* and *GND.* Input impedance *Rin* of an amplifier at DC must be small: *Rin = R1||R2* So *Rin must be much less* than *(Rbase = βRE) .* Here ‘much less than’*→ 0.1* is usually enough. Choose *R1 & R2* accordingly. For most BJT transistors you can take *β as ~ 200*

**Steps 5-7 : AC analysis: Gain of amplifier**

In forward bias mode the BE junction has an effective small internal resistance *re*given by the formula:

*Ω* where *IC* is expressed in mA …….. (*Eqn 1)*

***Step 5: Calculate the Gain G of the amplifier:***

The Gain of the CE amplifier at its quiet operating point is*: .....(Eqn 2)*

where 'little' re is the effective resistance at the base-emitter junction given by Eqn 1

Steps 6-7: A well-designed amplifier should not have any gain at DC (frequency = 0Hz). A non-zero gain at DC would imply any stray offset voltage at the input would be amplified and appear at the output superimposed on any amplified signal. We therefore set an *f3dB* frequency below which the amplifier’s gain decreases logarithmically.

The *f*3dB point is defined as the frequency where the gain decreases by a factor of 1/√2: in decibel units

this implies 20 log10(1/√2) ~ -3 dB

***Step 6: Determine C1­ based on desired lower frequency cutoff***

C1 in combination with the amplifier DC input resistance acts as a high-pass filter to block DC: The overall AC input impedance of the amplifier is the combination of parallel *R­1* & *R2* in parallel with *re* ‘seen through the BE junction’ with a multiplying factor *β*

*Rinp = (R1||R2) || β(re)*

***Step 7: Determine C2 based on desired lower cutoff:***

*C2* with *re* forms a second high-pass filter. Choose *C2* to satisfy the constraints of *f3dB*

**Part A: Design 5 marks**

**Design the circuit for a CE amplifier with the following operating parameters:**

***Part Amust be completed individually by each person – get it corrected before proceeding further***

a) *VCC* = 10V

b) *ICQ* = 1 mA

c) gain *G = -100* at quiet operating point

d) Amplifier lower cutoff frequency: f3dB = 100 Hz

Calculate the required component values in Fig 1 as per the design steps 1 – 7 and redraw your circuit here:

*There is a fundamental design limitation to this circuit – as discussed in the accompanying lecture.*

*In AC analysis, C2 short-circuits RE*

*So the gain is fixed at -RC/re*

*But re in turn is fixed by IC/25mV (with a little bit of temperature dependence, which is even worse)*

*The four parameters (a) – (d) above are artificially constructed to satisfy G = -RC/re*

*A realistic circuit design requires the addition of a gain setting resistor R3 in series with C2 as done in the next lab. Addition of R3 also introduces emitter feedback to stabilize the gain.*

**Part B: Build + Measure**

**Q1)** Build the circuit as per the design parameters you have calculated in Part A. Please be neat in your circuit connections and check your connections thrice (once by each group member!) – you have to make several intricate measurements below – it will be very difficult to debug a non-working circuit.

**2 marks**

**Q2)** Test your circuit’s operation by applying a very small amplitude of *Vin*< 20 mV.

Measure the gain *Vout/Vin* using the usual Y(t) and X-Y mode of the DSO. Verify that the circuit is working at the designed *ICQ*and exhibits the desired gain.

Draw the obtained *Vout/Vin* trace here **3 marks**

**Q3)** Frequency test. Perform the test of Q2 above at a few chosen frequencies in the range 1 kHz down to 100 Hz and check the dependence of the gain on the frequency. Demonstrate that the circuit behaves as expected with the *f3dB* lower cutoff at 100 Hz

[Plot the gain as a function of frequency here:] **2 marks**

**Q3)** [Difficulty: high] Now test your circuit’s performance with a larger amplitude of *Vin* > 20 mV

in the amplifier’s working frequency band of ~ 1 kHz

Observe *Vin* and *Vout*  in both Y(t)and X-Y mode.

Provide a hypothesis here to explain any unusual features you observe **3 marks**

**Space for Calculations**