**Laboratory Assignment 7 : Common Emitter Amplifier
with Feedback**

**Goal: [Complete Part A1 individually first before continuing further]**

In Lab 6, you set up a BJT in common-emitter (CE) mode without any form of feedback and a fixed gain determined by the bias point. Today, we will revisit the procedure and see how to design a for a specific gain value.

Fig 1 shows a CE amplifier with appropriate 'resistor-bias' circuit. The 7-step procedure to determine the component values is detailed below, as was discussed in the last lecture.

The exercises begin on Page 2.

Fig 1

C1

Function

Generator

**+**

**-**

R1

RC

R2

RE

R3

C2

Vcc

*Large Vout*

*Small Vin*

Fig 1

BJT CE Characteristics

from Lab 4
dashed line with descending slope indicates the
DC ‘load’ line.
*Vload = VCC – ICERC*

re

Vload

*Recall R3 was not present in Lab 6!*

20V

**The Design Process is split in two independent parts: First we do DC design to bias the BJT in Active mode. Then the AC design is done to make the amplifier amplify AC signals.**

**Steps 1 – 4 : DC Design:**

Capacitors block DC signals, so for this part, ignore all the capacitors. Capacitors are treated as open-circuit in DC analysis (i.e. no connection from one two terminals of the capacitor)

***Step 1: Choose the quiet operating point Q* *for IC*: *IQ***

*IQ* is given as an input to the design. The designer chooses *IQ* based on:

 a) desired power dissipation in the circuit – the amplifier will dissipate power *IQRC* at idle.

 b) load – how much current does the load connected to *Vload* need?

***Step 2: Choose RC***

We need to center *Vload* at the halfway point between *VCC* and ground. With *IC* from Step 1, this determines *Rc*

***Step 3: Choose RE***

Place *VE* at *~ 0.1VCC* for thermal stability of the transistor. Assume *IC=IE .*This determines *RE*

Note on input impedance ‘looking in’ from the base of the transistor: The impedance seen through the base of the transistor is the total resistance on the emitter side, amplified by the transistor’s *β:*

*Rbase =* *β(re+RE||R3).* In DC analysis, this reduces to *Rbase =* *β*(*re+RE*) ~ *βRE* ***Step 4: Determine R1 , R2 and R1/R2***For transistor to turn ON, *VBE* must be at least ~ 0.7V. Here we have already set *VE,* so VB must be *VE+0.7V* Assuming negligible current flow into base at DC (*~ μA*) determines the ratio R1/R2 as a voltage divider between *VCC* and *GND.* Input impedance of an amplifier at DC must be small, so we require *(Rin = R1||R2) << (Rbase = βRE)* . Here ‘much less than’*→ 0.1* is usually enough. Choose *R1* & *R2* accordingly. For most BJT transistors *β* is ~ 200

**Steps 5-7 : AC analysis: Gain of amplifier**

In forward bias mode the BE junction has an effective small internal resistance *re*given by the formula: $r\_{e}=\frac{25 mV}{I\_{C}}$ *Ω* ……….. (*Equation 1)* ( *IC* is expressed in mA in this equation)

***Step 5: Determine R3 to set desired gain G***The Gain of the CE amplifier at its quiet operating point is:$G= - \frac{R\_{c}}{r\_{e}+R\_{E}||R\_{3}}≈-\frac{R\_{c}}{r\_{e}+R\_{3}}$ *.....(Equation 2)*

where 'little' *re* is the resistance at the base-emitter junction given by Eqn 1

Typically *RE >> R3* so *RE* in parallel with *R3* can be approximated to a very good extent as *R3* in the denominator of Eqn 2. So the denominator reduces to *re+R3*

Steps 6-7: A well-designed amplifier should not have any gain at DC (frequency = 0Hz). A non-zero gain at DC would imply any stray offset voltage at the input would be amplified and appear at the output superimposed on any amplified signal. We therefore set an *f3dB* frequency below which the amplifier’s gain decreases logarithmically.

The *f*3dB point is defined as the frequency where the gain decreases by a factor of 1/√2: in decibel units

this implies 20 log10(1/√2) ~ -3 dB

***Step 6: Determine C1­ based on lower bandwidth limit:***

*C1* in combination with the amplifier DC input resistance acts as a high-pass filter to block DC: The overall input impedance of the amplifier is the combination of (*R­1* || *R2*) in parallel with (*re+RE||R3*)‘seen through the BE junction’ with a multiplying factor *β.* Using the same approximation as above (*RE||R3*) *~ R3,* we get:

 *Rinp = (R1||R2) || β(re+R3)*

*So:* $C\_{1}=\frac{1}{2πf\_{3dB} R\_{inp}}$

***Step 7: Determine C2 based on lower bandwidth limit:***

*C2* with (*re+RE||R3*)forms a second high-pass filter. Choose *C2* to satisfy the constraints of *f3dB*

*So:* *.................................................................................................(Eqn 3)*

Note that the two high pass filters calculated in steps 6 and 7 *each* decrease the gain by 3 dB at the *f3dB*point – so the net effect of both working together is to decrease the gain by *6 dB* at *f3dB*. You must take this into account while calculating *C1* and *C2*.

Point to ponder upon: Why are *C1* and *C2*both in the circuit?

**Part A: Design 5 marks**

**Design the circuit for a CE amplifier with the following operating parameters:**

***Part Amust be completed individually by each person – get it corrected before proceeding further. Space for calculations is provided on page 4 of this assignment sheet.***

a) *VCC* = 20V

b) *IQ* = 1 mA

c) AC gain *G = -50* at quiet operating point

d) Amplifier lower cutoff frequency: *f3dB* = 100 Hz.
 [Keep in mind the point made in Step 7 that *C­1* and *C2* each cause a 3dB reduction.

 – the overall amplifier design asks you to keep the total *f3dB* at 100 Hz.]

Calculate the required component values in Fig 1 as per the design steps 1 – 7.

In particular, calculate the value of AC gain in Step 5 for the two cases:

1. with *R3* absent, i.e. *R3* = 0 as in the previous Lab 6:
2. with *R3* present, and its value calculated as per Step 5

The answers to questions (a) and (b) should give you an idea of the relative importance of *R3* and *re* in setting the AC gain.

Redraw your circuit here with the calculated values of components.

**Part B: Build + Measure**

**Q1)** Build the circuit as per the design parameters you have calculated in Part A. Please be neat in your circuit connections and check your connections thrice (once by each group member!) – you must measure the DC values of voltages at all points in your circuit (*VE, VC, VB etc*)without any AC signal applied to verify that it conforms to the design calculations in Part A – there may be slight variation due to values of components used, but ensure that the transistor is biased to work in forward active mode.
You have to make several intricate measurements below – it will be very difficult to debug a non-working circuit.

 **2 marks**

**Q2)** AC Amplitude Test: Test your circuit’s operation by applying a small amplitude *Vin*< 0.2V.

 Measure the gain *Vout/Vin* using the usual Y(t) and X-Y mode of the DSO. Verify that the circuit is working at the designed *IQ*and exhibits the desired gain.

Draw the obtained *Vout/Vin* trace here **3 marks**

**Q3)** AC Frequency test: Perform the test of Q2 above at a few chosen frequencies in the range 1 kHz down to 50 Hz and check the dependence of the gain on the frequency. Demonstrate that the circuit behaves as expected with the *f3dB* lower cutoff at 100 Hz

[Plot the gain as a function of frequency here:] **2 marks**

**Q4)** AC Amplitude and linearity test Now test your circuit’s performance with a larger amplitude of *Vin* > 0.2 V in the amplifier’s working frequency band of ~ 1 kHz

Observe *Vin* and *Vout* in both Y(t)and X-Y mode.

You can use a triangular *Vin­* waveform to carefully measure the linearity of the gain or lack thereof, if any**.**  **3 marks**

***Space for Calculations***