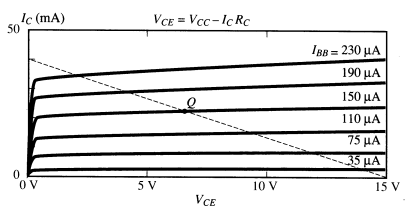
**Laboratory Assignment 8**

BJT CE Characteristics

and DC load line



*Large Vout*

**Marks: Q1: /1Q2: /1Q3: /1 Q4: /3 A: /3 B: /3 C: /3 Tot= /15**

Fig 1

**+**

**-**

*IRc*

Fig 1

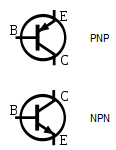
C1

Vcc

RL

Function

Generator



re

R1

R2

RC

RE

R3

C2

*IC*

*IL*

Note: we now account for load *RL* and *IL* explicitly unlike in previous labs

Vout

**CE Amplifer revised and improved**

**Goal: To improve the resistor-biased CE amplifier design of Labs 6,7**

In Labs6&7, we determined a step-by-step procedure for setting up the resistor bias network in a common emitter amplifier shown in Fig 1. A review of the steps is given on page 3.

Note that the design starts at step 1 with calculating the collector resistance R­c based on the operating point quiet collector current: it is determined by   
centering Vout­­­ between Vcc and 0V and taking into account   
the load’s current requirement.

DC load line for *RL → infinity*

20V

***It is never a good idea for a circuit design to ‘assume’ anything about the load it is going to drive: a good circuit should be able to drive ANY load***

In today’s lab assignment we will revise the design to make the CE design less dependent on the load characteristics.

***A key difference from earlier analyses is that the total current drawn from VCC through RC must account for both the transistor’s collector current IC and the load current IL :IRc= IC+IL***

*Answering the following questions will lead you to such a better design*

**Q1: Suppose Vcc = 20V and you start designing for a load resistance RL**

**In the middle of your experiment, RL suddenly decreases by to 0.8\*RL. Does VC change?**

**(choose from: increases/decreases/stays the same)**

**Q2: How does this change in RL affect your DC load line. How does the Q point change on the BJT characteristic with the new DC load line?**

**Q3: Given the answer to Q2 is your prior requirement for setting VC halfway between VCC and 0V guaranteed to be satisfied? If not, why not?**

**Q4: What change in the circuit would you make to ensure that VC does not change?**

*Hint: Note that in the straightforward design, the R1­ / R2dividerratio sets VB with respect to VCC. But in this case of changing load conditions, VCE is the important quantity – IL changes as the load changes, so VCE changes too! The quiet operating point Q on the amplifier’s IC v/s VCE characteristic changes as the load is changed. Only one of R1 or R2 should be needed to track the changing Q and apply ‘feedback’ so that IB adjusts itself accordingly. Remember that IC = βIB*

**Draw the modified circuit diagram here:**

*Note the distinction between IC (the collector current flowing into the transistor) and IRc – the total current across Rc which is shared by the load (IL) and the transistor’s collector (IC = βIB)*

**Part A: Design the circuit for a feedback biased CE amplifier as above with the following operating parameters:**

a) *IC* = 10 mA as the quiet operating point Q

b) *VCC* = 20V *VEE* = 0V

c) load *RL*= 10kΩ

d) Gain G = -20

d) Amplifier bandwidth: *f3dB* = 500 Hz

e) transistor *β = 200*

Mark the calculated component values in your diagram above.

**Part B: Build the circuit using the calculated values and demonstrate it's operation**

**Connect a load RL and measure Vout across R­L**

As usual,   
a) Check the DC voltages at various points in the circuit to verify that everything is working.

b) Use *V­in* as a triangular wave of frequency ~ 5 kHz to perform the AC measurement.  
Set *Vout*/*Vin*in X/Y mode on the DSO to calculate the gain and demonstrate that it matches the design gain.

**Part C: Test the Q point stability with changing *RL***

Change RL keeping the rest of the circuit same.

Re-measure the dc and ac characteristics of the amplifier as in Part B to determine if the Q point of the circuit has changed and/or the gain is affected.

Try values like 0.75\*RL , 1.25\*RL­  and a few others to determine at what point the amplifier’s feedback bias is unable to compensate for the changing load resistance.

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**CE Design procedure with collector feedback bias – revision of design steps with a few important modifications to assumptions**

**Steps 1-4: DC Design: Set Q point and bias the amplifer in forward active mode**

Capacitors block DC signals, so for DC analysis, all the capacitors are treated as open-circuit

***Step 1: Choose the quiet operating point Q:***

*Choice of Ic is usually an input to the design governed by two things:*

*a) power dissipation in the circuit – remember this is the current that the transistor will draw at 'idle'*

*b) Load line – the amplifier’s must always remain linear (the transistor must not go into saturation or cutoff)*

***Step 2: Choose RC***

*We need to center Vout at the halfway point between VCC and ground. Ic is takenfrom Step 1 and load current requirement IL­ is set by RL. VC = VL* *­ and VC set at 0.5VCC . With IRc=IC + IL you can determine Rc*

***Step 3: Choose RE***

*Place VE at ~ 0.1Vcc  for thermal stability of the transistor. Assume IC=IE . This determines RE*

***Step 4: Bias the transistor in Forward Active mode [this step is different from the resistor divider bias we worked on earlier]***

*For transistor to turn ON, VBE must be at least ~ 0.7V. Here we have already set VE in Step 3,  
 so VB must be VE+ 0.7V. Assume negligible current flow into base at DC (~ μA). Ic is known from Step 1.   
You will have determined a clever simplification of the biasing circuit in answering Question 4 of this assignment. In solving KVL for the base emitter loop with a simplified biasing scheme, you will need to use the relations IE=(β+1)IB , IC=βIB and IC ~ IE (IB ­is μA!)*

**Steps 5-7 : AC analysis: Gain of amplifier**

*R3 primarily determines the AC gain of the CE amplifier (Not β ! which determines the input impedance at DC)*

***Step 5: Determine R3 to set desired gain G***

*The Gain of the CE amplifier at its quiet operating point is : ................................(Eqn 1)  
 where 'little' re is the temperature-dependent resistance at the base-emitter junction given approximately by: Ω…………................................(Eqn 2)*

*Note the appearance of RL in the numerator of the gain equation – in earlier designs we connected the DSO probe as the load with effectively infinite RL ~ MΩ*

*~~Typically R~~~~E~~~~>>R~~~~3~~ ~~so R~~~~E~~ ~~in parallel with R~~~~3~~ ~~can be approximated to a very good extent as R~~~~3~~ ~~in the denominator of Eqn 1 which therefore reduces to (r~~~~e~~ ~~+ R~~~~3~~~~)~~*

*It is now not justified to make to make the simplification that RE >> R3 in Eqn 1. Eqn 1 is linear with G(specified) and RC, RL , re , RE known – so you can solve it to obtain R3*

***Step 6: Determine C2 based on desired bandwidth of signal amplification:***

*To determine C2 the relevant resistance for the high-pass RC filter is R ~ (re + R3) as from Eqn 1 above*

*So:* *............................................................................................................(Eqn 3)*

***Step 7: Determine C1:***

*C1 in combination with the amplifier’s DC input resistance acts as a second high-pass filter to block DC*

*So: ……………………………………………………………………..………….(Eqn 4)  
Rin for the complete circuit worked out in Question 4 will be:  
Rin =* [ *RB + RC||RL* ] | | [ *β* (*re + RE||R3*) ]   
*where the first term comes from the collector feedback bias circuit and the second term from the emitter leg.*

**Space for calculations**