**Laboratory Assignment 10**

**Marks: A: /3 B: /5 C: /2+3+2 Tot= /15**

**Emitter Follower as a transistor current amplifier**

Exercises begin on Page 2.

**Summary** of Labs 5,6,7,8-9: We worked with the NPN BJT as a *voltage controlled voltage source VCVS.*Here are the main points we learnt in Lab in the past labs:

* The transistor *turns on* when the B-E junction is forward biased i.e. *VBE> 0.7V*
* The transistor must be operated by setting up a bias circuit so that it remains in the ‘Forward-Active’ region of its characteristic as. The three regions of the characteristic are:
  + Cutoff:*VBE*falls below 0.7V and the transistor is effectively off.
  + Forward-Active: When *0.1VCC< VCE< VCC*­, B-E junction is forward biased and C-B junction is reverse biased. In this region the transistor works as a linear amplifier with *IC = βIB*, *β ~ 100*Note that you should not think of the collector *current* as current due to *diode conduction.* This is because C-B junction normally has reverse bias voltage applied across it.
  + Saturation:When*VCE*<*0.25V*, the transistor acts as a ‘switch’ By varying *IB* the transistor can be made to switch rapidly between cutoff (off) and forward-active (on).
* Amplifier circuit design requires you to place the stable operating point at a suitable point in the forward-active region by applying the appropriate bias voltages to the CB and BE junctions.   
  Simple resistor-divider biasing network is shown in Fig 1b [as used in Lab 6]  
  Other biasing circuits are also possible that automatically compensate for load variation [Labs 8,9 – collector feedback bias]  
  Today we will work with the simple resistor divider bias.
* The transistor in Forward-Active mode can be regarded as a little can with a sailor inside it as shown in the cartoon in Fig 1c: The sailor’s job is to keep looking at *IB­*and ‘steer’ *IC* so that *IC = βIB*  
  The sailor’s working conditions are that the transistor must be biased in forward active mode, i.e*VBE>0.7V* and*VCE> 0.25V­*

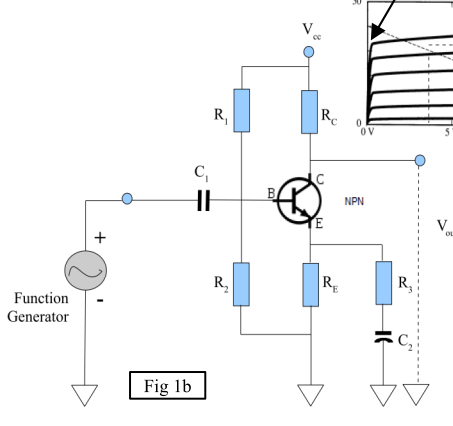


Fig 1b: Emitter Follower

(resistor divider bias)

RL

C2

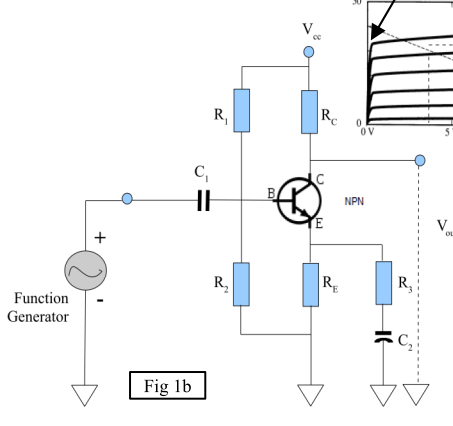
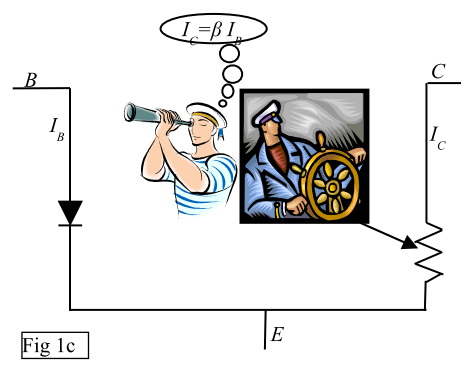


Fig 1a: CE amplifier

(resistor divider bias)

*Vin*



All the circuits we designed so far extracted the output from the collector of the transistor.

In this lab, we will extract the output from the emitter where *IE ~ IC* is the amplified current.

**Design steps for an emitter follower:**

As discussed in the last lecture, the steps for designing an Emitter follower are very similar to thoseused for a CE voltage amplifier – in fact some of the steps are simpler.

***Step 1: Choose to draw the output from the emitter instead of the collector***

a) In common collector mode, Collector is directly connected to *VCC* omitting *RC*

b) *C2* acts as a decoupling capacitor to the load resistance *RL*

***Step 2: Choose the quietoperating point Q for the collector current: IQ***

Choice of *IQ*is governed by the load *–* how much maximum RMS power does the load *RL*need? The maxiumum RMS power is given by *(2IQ)2R­L/8*

***Step 3: Choose RE***

*RE* is calculated to place *VE*at the center between *VCC* and 0.

***Step 4: Determine bias resistors R1&R2***

Choose *R1*and *R2*to set*VB*at *~ VE+0.7V*

The ratio *R1/R2* acts as a voltage divider between *VCC*and *GND.* For negligible current flow into base at DC  
we must satisfy  *(R1||R2) <<Rbase = β(re+RE) . Here ‘much less than’→ 0.1 is usually enough.*

***Step 5: Determine C1 C2 :***

*In combination with the amplifier DC input resistance, C1 acts as a high-pass filter to block low frequencies:*

*Rinp = (R1||R2) || β(re+RE*||*RL) where re = 25mV/IQ*

*So:   
 C2* is determined similarly taking the resistors in the emitter leg into account (be careful of making approximations!)

**Part A: Design**

Suppose you like to listen to music at ear-splittingly loud volume on your headphones.

1. Measure the dc load resistance of each of the left & right channel in yourheadphones. A 3.8mm stereo headphone connector has three connector bands: by convention, the Tip is left channel, the middleRing is right channel and outer Sleeve is ground. (this is called the TRS convention). For a hands-free headset type headphone, there is a fourth band TRS+Mic.  
   Your *RL = ~ 15 to 50Ω for most headphones*
2. Let us assume that 10 mW of power is adequate to drive the headphone to ear-splitting loud volume.

The answers to Q1 and Q2 determine your *RL* and load power requirements as input to your design.

For uniformity (and safety of your headphones), we will work with a dummy load resistor *RL =* 200Ω

Let us further assume that your amplifier is built into your cellphone, so we are working with *VCC=5V*

Design an emitter follower *current* amplifier with a transistor of *β=100* as outlined in steps 1 to 5 above. Use *f3dB* =4000 Hz (so you will miss out most of the ‘bass’ parts of an audio signal which are not good for your health anyway!)

Calculate the bias resistors and input/output decoupling capacitor values

*(2IQ2)/8 \* 200 = 10 mW → IQ = 10 mA; re=2.5Ω RE = 2.5V/IQ → RE = 250Ω*

*R1 & R2 calculated as usual: R1 = 4kΩ R2 = 7kΩ*

**Part B: Circuit building**

Build the circuit designed in part A and demonstrate its operation with a triangle input signal. In particular, check if the voltage at the circuit output *VE* is able to swing through the full range between ~0 and *VCC*

**Part C: Analysis**

1. What is the power dissipated by your circuit when *no input signal* is present *Vin=0*? i.e., the circuit is idle with no input.  
   The amplifier circuit consists of the BJT, RE, R1, R2, C1, C2The load RL is to be considered as a separate component.  
   Calculate:  
   1. Power dissipated in Amplifier circuit at idle: *Pbias(R1+R2)* + *PRE*  + *Ptrans(VCE\*IQ) = 53mW*  
       *PBE can be neglected due to µA IB* *PRE + Ptrans make up the bulk of the waste power dissipation at idle*
   2. Power dissipated in Load RL at idle: 0
2. Applying a triangular input signal *Vin* , observe carefully the *voltage* gain *VL/Vin*: ~ 1
   1. What is the maximum amplitude of *Vin* you can apply before *Vout* distorts
   2. What is the *current* gain *IL/Iin ? ~ 10*
   3. What is the power dissipated in the amplifier circuit and Load RL at max loud output:  
      *See page 4+5 for detailed calculations.  
      based on observed vin = 2.35Vpp & v­out=2.25pp  
      Total power dissipated in amp circuit = Pdc + Pac = 53 mW + 5.7 mW  
      Total power delivered to load = 2.19 mW*

In both cases, what is the ratio of useful power delivered to load over the power dissipated as heat within the amplifier circuit? ~ 3.7%

1. Does this make the simple emitter follower a viable current amplifier to use in your cellphone? With a 4000mAh battery in the cellphone, calculate how long the battery would last if you were to play music at maximum loudness continuously with the headphones driven by this emitter follower (assuming you are using the device for exclusively listening to music without any phone calls)

5V \* 4000 mA-hr = 20W-hr capacity 20 W-hr/(58.7mW amp + 2.19mW load)(consumption) = 330 hrs

