Name: *Roll#*

Laboratory Assignment 6 : Common Emitter Amplifier

Marks **A:** /5 **B_1:** /2 **B_2:** /3 **B_3:** /2 **B_4:** /3 **Tot=** /15

Goal: [Complete Part A_1 individually first before continuing further]

In Lab 5, you set up a BJT in common-emitter (CE) mode and found the associated passive components to be added to the circuit mostly by trial/error/consultation. Today we will go through a systematic procedure of how to 'bias' the transistor so that it behaves linearly as an amplifier.
Fig 1 shows a CE amplifier with appropriate 'resistor-bias' circuit. The 7-step procedure to determine the component values is detailed below. The exercises begin on Page 2.

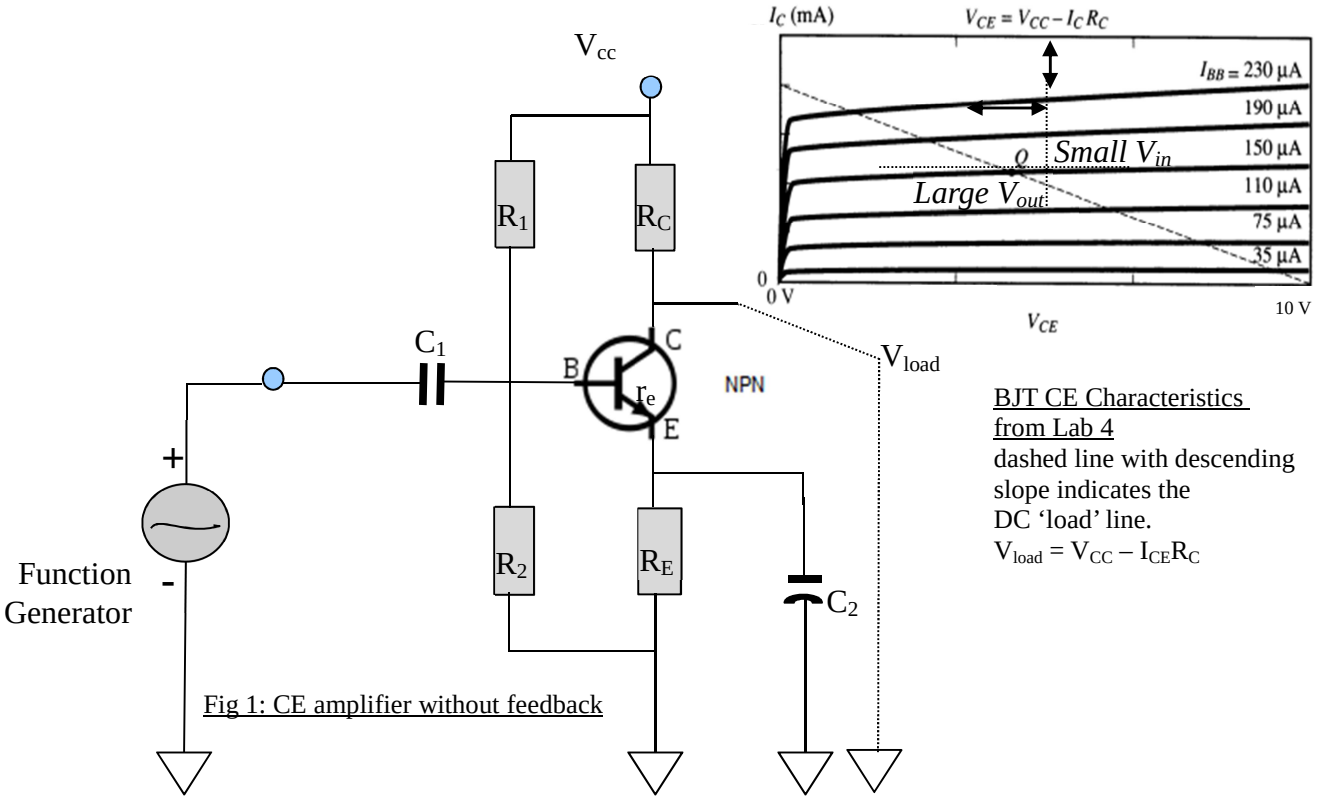

Fig 1: CE amplifier without feedback

BJT CE Characteristics from Lab 4
dashed line with descending slope indicates the DC 'load' line.
$V_{load} = V_{CC} - I_{CE}R_C$

The Design Process is split in two independent parts: First we do DC design to bias the BJT in Active mode, then the AC design is done to make the amplifier amplify AC signals

Steps 1 – 4 : DC Design:

Capacitors block DC signals, so for this part, ignore all the capacitors. Capacitors are treated as open-circuit in DC analysis (i.e. no connection from one two terminals of the capacitor)

Step 1: Choose the quiet operating point Q for I_C: I_{CQ}

I_{CQ} is given as an input to the design. The designer chooses I_{CQ} based on:
a) desired power dissipation in the circuit – the amplifier will dissipate power $I_{CQ}R_C$ at idle.
b) load – how much current does the load connected to V_{load} need?

Step 2: Choose R_C

We need to center V_{load} at the halfway point between V_{CC} and ground. With I_C from Step 1, this determines R_c

Step 3: Choose R_E

Place V_E at ~ *1V* for thermal stability of the transistor. Assume $I_C = I_E$ This determines R_E

Step 4: Determine R_1 and R_2

For transistor to be in active mode, V_{BE} must be at least *0.6V.* Here we have already set V_E at *1V,* so V_B must be *1.6V.* Assuming negligible current flow into base at DC determines the ratio R_1/R_2 as a voltage divider between V_{CC} and *GND.* Input impedance R_{in} of an amplifier at DC must be small: $R_{in} = R_1||R_2$ So R_{in} *must be much less* than $(R_{base} = \beta R_E)$. Here 'much less than'→ *0.1* is usually enough. Choose R_1 & R_2 accordingly.
For most BJT transistors you can take β *as ~ 200*

Steps 5-7 : AC analysis: Gain of amplifier

In forward bias mode the BE junction has an effective small internal resistance r_e given by the formula:
$r_e = \frac{25\ mV}{I_C}\ \Omega$ where I_C is expressed in mA …….. *(Eqn 1)*

Step 5: Calculate the Gain G of the amplifier:

The Gain of the CE amplifier at its quiet operating point is*:* $G = -\frac{R_c}{r_e}$ *.....(Eqn 2)*
where 'little' r_e is the effective resistance at the base-emitter junction given by Eqn 1

Steps 6-7: A well-designed amplifier should not have any gain at DC (frequency = 0Hz). A non-zero gain at DC would imply any stray offset voltage at the input would be amplified and appear at the output superimposed on any amplified signal. We therefore set an f_{3dB} frequency below which the amplifier's gain decreases logarithmically. The f_{3dB} point is defined as the frequency where the gain decreases by a factor of 1/√2: in decibel units this implies $20 \log_{10}(1/\sqrt{2}) \sim -3$ dB

Step 6: Determine C_1 based on desired lower frequency cutoff

C_1 in combination with the amplifier DC input resistance acts as a high-pass filter to block DC: The overall AC input impedance of the amplifier is the combination of parallel R_1 & R_2 in parallel with r_e 'seen through the BE junction' with a multiplying factor β

$R_{inp} = (R_1||R_2)\ ||\ \beta(r_e)$

$C_1 = \frac{1}{2\pi f_{3dB} R_{inp}}$

Step 7: Determine C_2 based on desired lower cutoff:

C_2 with r_e forms a second high-pass filter. Choose C_2 to satisfy the constraints of f_{3dB}

$C_2 = \frac{1}{2\pi f_{3dB} r_e}$

Part A: Design 5 marks

Design the circuit for a CE amplifier with the following operating parameters:
Part A must be completed individually by each person – get it corrected before proceeding further

a) V_{CC} = 10V
b) I_{CQ} = 1 mA
c) gain G = *-100* at quiet operating point
d) Amplifier lower cutoff frequency: f_{3dB} = 100 Hz

Calculate the required component values in Fig 1 as per the design steps 1 – 7 and redraw your circuit here:

Part B: Build + Measure

Q1) Build the circuit as per the design parameters you have calculated in Part A. Please be neat in your circuit connections and check your connections thrice (once by each group member!) – you have to make several intricate measurements below – it will be very difficult to debug a non-working circuit.
2 marks

Q2) Test your circuit's operation by applying a very small amplitude of V_{in} < 20 mV.
Measure the gain V_{out}/V_{in} using the usual Y(t) and X-Y mode of the DSO. Verify that the circuit is working at the designed I_{CQ} and exhibits the desired gain.
Draw the obtained V_{out}/V_{in} trace here **3 marks**

Q3) Frequency test. Perform the test of Q2 above at a few chosen frequencies in the range 1 kHz down to 100 Hz and check the dependence of the gain on the frequency. Demonstrate that the circuit behaves as expected with the f_{3dB} lower cutoff at 100 Hz
[Plot the gain as a function of frequency here:] **2 marks**

Q3) [Difficulty: high] Now test your circuit's performance with a larger amplitude of V_{in} > 20 mV in the amplifier's working frequency band of ~ 1 kHz
Observe V_{in} and V_{out} in both Y(t)and X-Y mode.
Provide a hypothesis here to explain any unusual features you observe **3 marks**

Space for Calculations