Name: *Roll#*

Laboratory Assignment 7 : Common Emitter Amplifier with Feedback

Goal: [Complete Part A_1 individually first before continuing further]

In Lab 6, you set up a BJT in common-emitter (CE) mode without any form of feedback and a fixed gain determined by the bias point. Today, we will revisit the procedure and see how to design a for a specific gain value.

Fig 1 shows a CE amplifier with appropriate 'resistor-bias' circuit. The 7-step procedure to determine the component values is detailed below, as was discussed in the last lecture.

The exercises begin on Page 2.

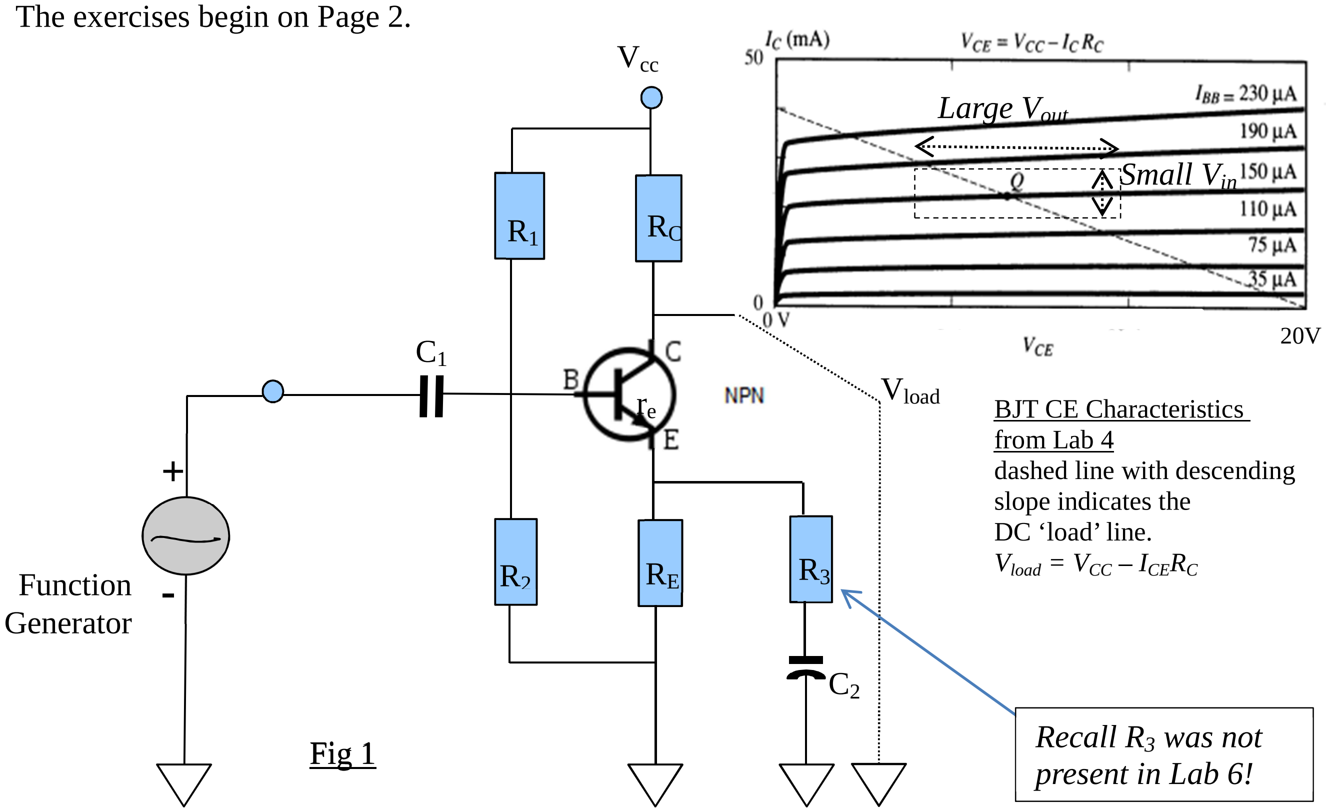

Fig 1

BJT CE Characteristics from Lab 4

dashed line with descending slope indicates the DC 'load' line.

$V_{load} = V_{CC} - I_{CE}R_C$

Recall R_3 was not present in Lab 6!

The Design Process is split in two independent parts: First we do DC design to bias the BJT in Active mode. Then the AC design is done to make the amplifier amplify AC signals.

Steps 1 – 4 : DC Design:

Capacitors block DC signals, so for this part, ignore all the capacitors. Capacitors are treated as open-circuit in DC analysis (i.e. no connection from one two terminals of the capacitor)

Step 1: Choose the quiet operating point Q for I_C: I_Q

I_Q is given as an input to the design. The designer chooses I_Q based on:

a) desired power dissipation in the circuit – the amplifier will dissipate power $I_Q R_C$ at idle.

b) load – how much current does the load connected to V_{load} need?

Step 2: Choose R_C

We need to center V_{load} at the halfway point between V_{CC} and ground. With I_C from Step 1, this determines R_c

Step 3: Choose R_E

Place V_E at ~ $0.1V_{CC}$ for thermal stability of the transistor. Assume $I_C=I_E$. This determines R_E

Note on input impedance 'looking in' from the base of the transistor: The impedance seen through the base of the transistor is the total resistance on the emitter side, amplified by the transistor's β: $R_{base} = \beta(r_e+R_E||R_3)$. In DC analysis, this reduces to $R_{base} = \beta(r_e+R_E) \sim \beta R_E$

Step 4: Determine R_1 , R_2 and R_1/R_2

For transistor to turn ON, V_{BE} must be at least ~ 0.7V. Here we have already set V_E, so V_B must be $V_E+0.7V$
Assuming negligible current flow into base at DC (~ μA) determines the ratio R_1/R_2 as a voltage divider between V_{CC} and *GND*. Input impedance of an amplifier at DC must be small, so we require $(R_{in} = R_1||R_2) << (R_{base} = \beta R_E)$. Here 'much less than'→ *0.1* is usually enough. Choose R_1 & R_2 accordingly.
For most BJT transistors β is ~ 200

Steps 5-7 : AC analysis: Gain of amplifier

In forward bias mode the BE junction has an effective small internal resistance r_e given by the formula:
$r_e = \frac{25\,mV}{I_C}\,\Omega$ ……….. (*Equation 1)* (I_C is expressed in mA in this equation)

Step 5: Determine R_3 to set desired gain G

The Gain of the CE amplifier at its quiet operating point is: $G = -\frac{R_C}{r_e+R_E||R_3} \approx -\frac{R_C}{r_e+R_3}$ .....*(Equation 2)*

where 'little' r_e is the resistance at the base-emitter junction given by Eqn 1

Typically $R_E >> R_3$ so R_E in parallel with R_3 can be approximated to a very good extent as R_3 in the denominator of Eqn 2. So the denominator reduces to r_e+R_3

Steps 6-7: A well-designed amplifier should not have any gain at DC (frequency = 0Hz). A non-zero gain at DC would imply any stray offset voltage at the input would be amplified and appear at the output superimposed on any amplified signal. We therefore set an f_{3dB} frequency below which the amplifier's gain decreases logarithmically.
The f_{3dB} point is defined as the frequency where the gain decreases by a factor of $1/\sqrt{2}$: in decibel units this implies $20 \log_{10}(1/\sqrt{2}) \sim -3$ dB

Step 6: Determine C_1 based on lower bandwidth limit:

C_1 in combination with the amplifier DC input resistance acts as a high-pass filter to block DC: The overall input impedance of the amplifier is the combination of ($R_1 || R_2$) in parallel with ($r_e+R_E||R_3$) 'seen through the BE junction' with a multiplying factor β. Using the same approximation as above ($R_E||R_3$) ~ R_3, we get:

$R_{inp} = (R_1||R_2) || \beta(r_e+R_3)$

So: $C_1 = \frac{1}{2\pi f_{3dB}\, R_{inp}}$

Step 7: Determine C_2 based on lower bandwidth limit:

C_2 with ($r_e+R_E||R_3$) forms a second high-pass filter. Choose C_2 to satisfy the constraints of f_{3dB}

So: $C_2 = \frac{1}{2\pi f_{3dB}(r_e+R_3)}$ ....*(Eqn 3)*

Note that the two high pass filters calculated in steps 6 and 7 *each* decrease the gain by 3 dB at the f_{3dB} point – so the net effect of both working together is to decrease the gain by *6 dB* at f_{3dB}. You must take this into account while calculating C_1 and C_2.
Point to ponder upon: Why are C_1 and C_2 both in the circuit?

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Part A: Design 5 marks

Design the circuit for a CE amplifier with the following operating parameters:

Part A must be completed individually by each person – get it corrected before proceeding further. Space for calculations is provided on page 4 of this assignment sheet.

a) V_{CC} = 20V
b) I_Q = 1 mA
c) AC gain $G = -50$ at quiet operating point
d) Amplifier lower cutoff frequency: f_{3dB} = 100 Hz.
[Keep in mind the point made in Step 7 that C_1 and C_2 each cause a 3dB reduction.
– the overall amplifier design asks you to keep the total f_{3dB} at 100 Hz.]

Calculate the required component values in Fig 1 as per the design steps 1 – 7.
In particular, calculate the value of AC gain in Step 5 for the two cases:

a) with R_3 absent, i.e. $R_3 = 0$ as in the previous Lab 6:

b) with R_3 present, and its value calculated as per Step 5

The answers to questions (a) and (b) should give you an idea of the relative importance of R_3 and r_e in setting the AC gain.
Redraw your circuit here with the calculated values of components.

Part B: Build + Measure

Q1) Build the circuit as per the design parameters you have calculated in Part A. Please be neat in your circuit connections and check your connections thrice (once by each group member!) – you must measure the DC values of voltages at all points in your circuit (V_E, V_C, V_B *etc*) without any AC signal applied to verify that it conforms to the design calculations in Part A – there may be slight variation due to values of components used, but ensure that the transistor is biased to work in forward active mode.
You have to make several intricate measurements below – it will be very difficult to debug a non-working circuit.

2 marks

Q2) AC Amplitude Test: Test your circuit's operation by applying a small amplitude $V_{in} < 0.2$V. Measure the gain V_{out}/V_{in} using the usual Y(t) and X-Y mode of the DSO. Verify that the circuit is working at the designed I_Q and exhibits the desired gain.
Draw the obtained V_{out}/V_{in} trace here **3 marks**

Q3) AC Frequency test: Perform the test of Q2 above at a few chosen frequencies in the range 1 kHz down to 50 Hz and check the dependence of the gain on the frequency. Demonstrate that the circuit behaves as expected with the f_{3dB} lower cutoff at 100 Hz
[Plot the gain as a function of frequency here:] **2 marks**

Q4) AC Amplitude and linearity test Now test your circuit's performance with a larger amplitude of V_{in} > 0.2 V in the amplifier's working frequency band of ~ 1 kHz
Observe V_{in} and V_{out} in both Y(t)and X-Y mode.
You can use a triangular V_{in} waveform to carefully measure the linearity of the gain or lack thereof, if any. **3 marks**

Space for Calculations