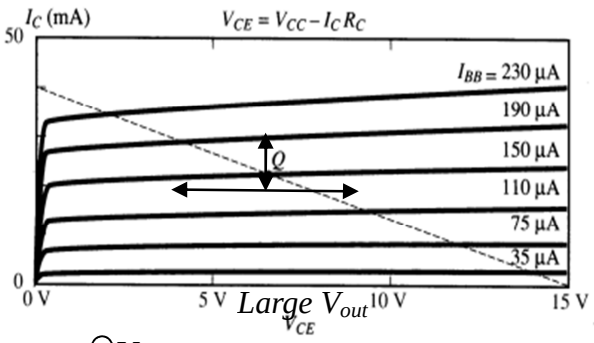
Name: *Roll#*

Marks: Q_1: /1 Q_2: /1 Q_3: /1 Q_4: /3 A: /3 B: /3 C: /3 Tot= /15

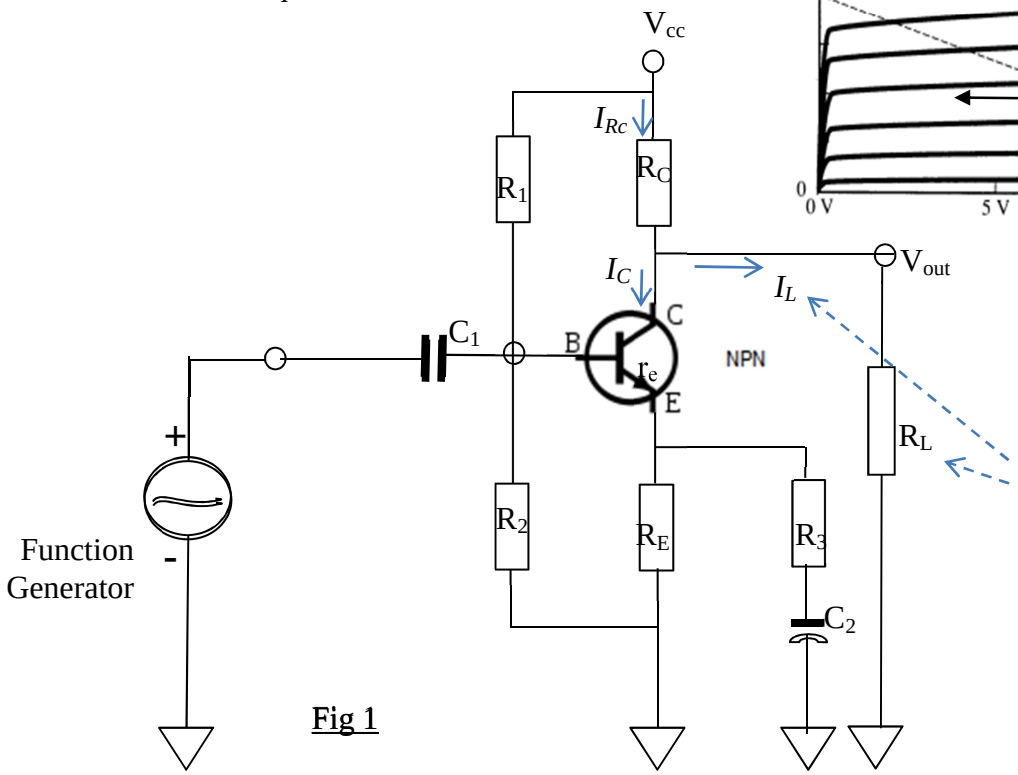
Laboratory Assignment 8
CE Amplifer revised and improved

Goal: <u>To improve the resistor-biased CE amplifier design of Labs 6,7</u>

In Labs6&7, we determined a step-by-step procedure for setting up the resistor bias network in a common emitter amplifier shown in Fig 1. A review of the steps is given on page 3.
Note that the design starts at step 1 with calculating the collector resistance R_c based on the operating point quiet collector current: it is determined by centering V_{out} between V_{cc} and 0V and taking into account the load's current requirement.



BJT CE Characteristics and DC load line



Note: we now account for load R_L and I_L explicitly unlike in previous labs

Fig 1

<u>It is never a good idea for a circuit design to 'assume' anything about the load it is going to drive: a good circuit should be able to drive ANY load</u>

In today's lab assignment we will revise the design to make the CE design less dependent on the load characteristics.
A key difference from earlier analyses is that the total current drawn from V_{CC} through R_C must account for both the transistor's collector current I_C and the load current I_L :I_{Rc}= I_C+I_L
Answering the following questions will lead you to such a better design

<u>Q1:</u> Suppose V_{cc} = 20V and you start designing for a load resistance R_L
In the middle of your experiment, R_L suddenly decreases by to 0.8*R_L. Does V_C change? (choose from: increases/decreases/stays the same)

<u>Q2:</u> How does this change in R_L affect your DC load line. How does the Q point change on the BJT characteristic with the new DC load line?

Q3: Given the answer to Q2 is your prior requirement for setting V_C halfway between V_{CC} and 0V guaranteed to be satisfied? If not, why not?

Q4: What change in the circuit would you make to ensure that V_C does not change?
Hint: Note that in the straightforward design, the R_1 / R_2dividerratio sets V_B with respect to V_{CC}. But in this case of changing load conditions, V_{CE} is the important quantity – I_L changes as the load changes, so V_{CE} changes too! The quiet operating point Q on the amplifier's I_C v/s V_{CE} characteristic changes as the load is changed. Only one of R_1 or R_2 should be needed to track the changing Q and apply 'feedback' so that I_B adjusts itself accordingly. Remember that $I_C = \beta I_B$
Draw the modified circuit diagram here:
Note the distinction between I_C (the collector current flowing into the transistor) and I_{Rc} – the total current across R_c which is shared by the load (I_L) and the transistor's collector ($I_C = \beta I_B$)

Part A: Design the circuit for a feedback biased CE amplifier as above with the following operating parameters:

a) I_C = 10 mA as the quiet operating point Q
b) V_{CC} = 20V V_{EE} = 0V
c) load R_L= 10kΩ
d) Gain G = -20
d) Amplifier bandwidth: f_{3dB} = 500 Hz
e) transistor $\beta = 200$
Mark the calculated component values in your diagram above.

Part B: Build the circuit using the calculated values and demonstrate it's operation

Connect a load R_L and measure V_{out} across R_L

As usual,

a) Check the DC voltages at various points in the circuit to verify that everything is working.

b) Use V_{in} as a triangular wave of frequency ~ 5 kHz to perform the AC measurement.

Set V_{out}/V_{in} in X/Y mode on the DSO to calculate the gain and demonstrate that it matches the design gain.

Part C: Test the Q point stability with changing R_L

Change R_L keeping the rest of the circuit same.

Re-measure the dc and ac characteristics of the amplifier as in Part B to determine if the Q point of the circuit has changed and/or the gain is affected.

Try values like $0.75*R_L$, $1.25*R_L$ and a few others to determine at what point the amplifier's feedback bias is unable to compensate for the changing load resistance.

CE Design procedure with collector feedback bias – revision of design steps with a few important modifications to assumptions

Steps 1-4: DC Design: Set Q point and bias the amplifer in forward active mode

Capacitors block DC signals, so for DC analysis, all the capacitors are treated as open-circuit

Step 1: Choose the quiet operating point Q:

Choice of I_c is usually an input to the design governed by two things:

a) power dissipation in the circuit – remember this is the current that the transistor will draw at 'idle'

b) Load line – the amplifier's must always remain linear (the transistor must not go into saturation or cutoff)

Step 2: Choose R_C

We need to center V_{out} at the halfway point between V_{CC} and ground. I_c is taken from Step 1 and load current requirement I_L is set by R_L. $V_C = V_L$ and V_C set at $0.5V_{CC}$. With $I_{Rc}=I_C + I_L$ you can determine R_c

Step 3: Choose R_E

Place V_E at ~ $0.1V_{cc}$ for thermal stability of the transistor. Assume $I_C=I_E$. This determines R_E

Step 4: Bias the transistor in Forward Active mode [this step is different from the resistor divider bias we worked on earlier]

For transistor to turn ON, V_{BE} must be at least ~ 0.7V. Here we have already set V_E in Step 3, so V_B must be V_E+ 0.7V. Assume negligible current flow into base at DC (~ μA). I_c is known from Step 1. You will have determined a clever simplification of the biasing circuit in answering Question 4 of this assignment. In solving KVL for the base emitter loop with a simplified biasing scheme, you will need to use the relations $I_E=(\beta+1)I_B$, $I_C=\beta I_B$ and $I_C \sim I_E$ (I_B is μA!)

Steps 5-7 : AC analysis: Gain of amplifier

R_3 primarily determines the AC gain of the CE amplifier (Not β ! which determines the input impedance at DC)

Step 5: Determine R_3 to set desired gain G

The Gain of the CE amplifier at its quiet operating point is : $G = -\frac{R_C||R_L}{r_e+R_E||R_3}$ *.....(Eqn 1)*

where 'little' r_e is the temperature-dependent resistance at the base-emitter junction given approximately by:

$r_e = \frac{25\ mV}{I_C(mA)}\ \Omega$ *.....(Eqn 2)*

Note the appearance of R_L in the numerator of the gain equation – in earlier designs we connected the DSO probe as the load with effectively infinite R_L ~ MΩ

~~*Typically R_E>>R_3 so R_E in parallel with R_3 can be approximated to a very good extent as R_3 in the denominator of Eqn 1 which therefore reduces to (r_e + R_3)*~~

It is now not justified to make to make the simplification that R_E >> R_3 in Eqn 1. Eqn 1 is linear with G(specified) and R_C, R_L , r_e , R_E known – so you can solve it to obtain R_3

Step 6: Determine C_2 based on desired bandwidth of signal amplification:

To determine C_2 the relevant resistance for the high-pass RC filter is R ~ (r_e + R_3) as from Eqn 1 above

So: $C_2 = \frac{1}{2\pi f_{3dB}(r_e + R_3)}$ *.....(Eqn 3)*

Step 7: Determine C_1:

C_1 in combination with the amplifier's DC input resistance acts as a second high-pass filter to block DC

So: $C_1 = \frac{1}{2\pi f_{3dB} R_{in}}$ *.....(Eqn 4)*

R_{in} for the complete circuit worked out in Question 4 will be:

R_{in} = [R_B + $R_C||R_L$] | | [β (r_e + $R_E||R_3$)]

where the first term comes from the collector feedback bias circuit and the second term from the emitter leg.

Space for calculations