EP215
Electronics Lab 1

Lecture 4

Review of Lab 3: I-V characteristics
and stray effects

What is special about the differential input test setup?

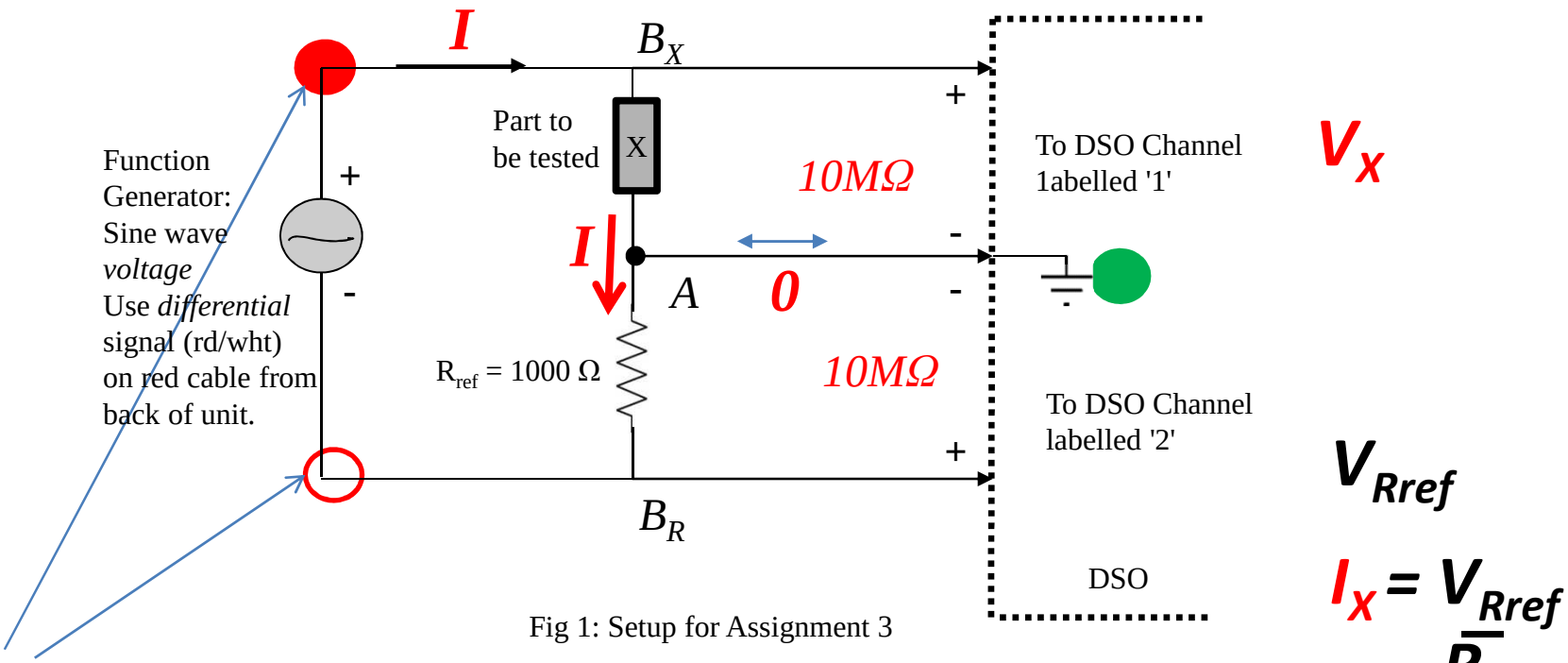


Fig 1: Setup for Assignment 3

Input signal at these points
Must not refer to **GND** potential

What is special about the differential input test setup?

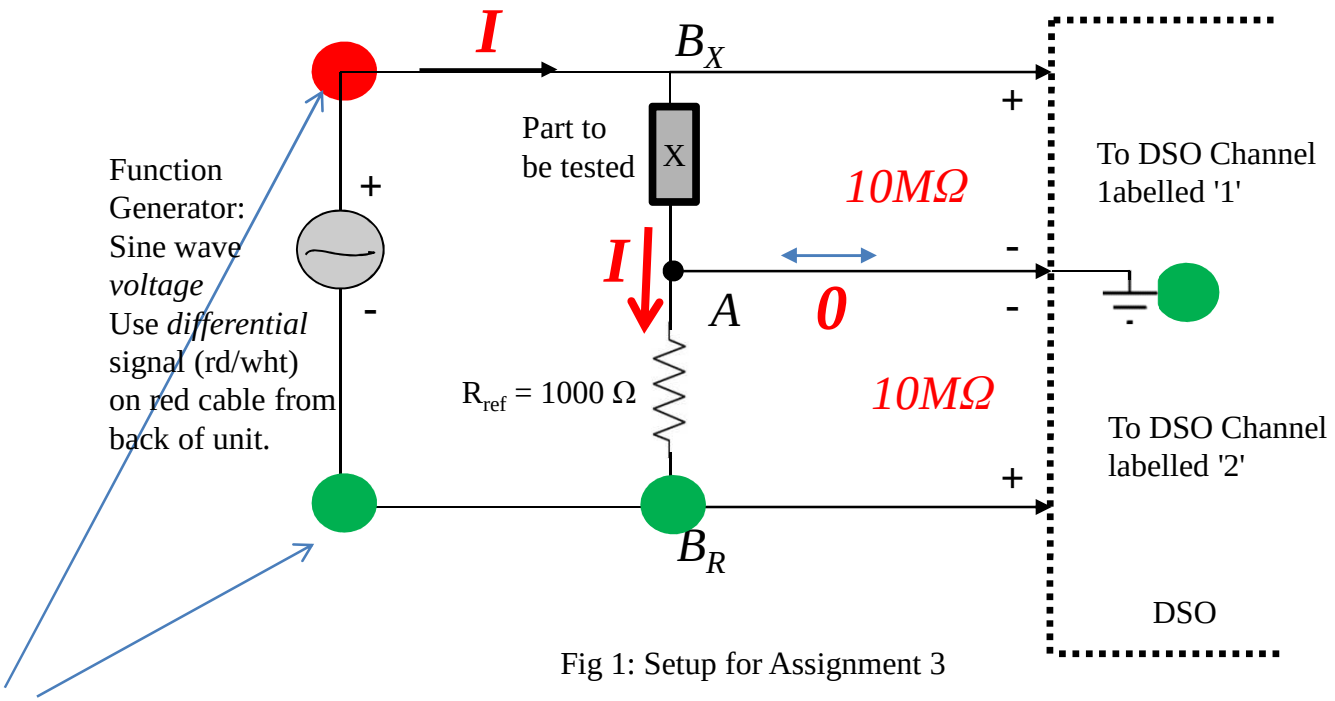
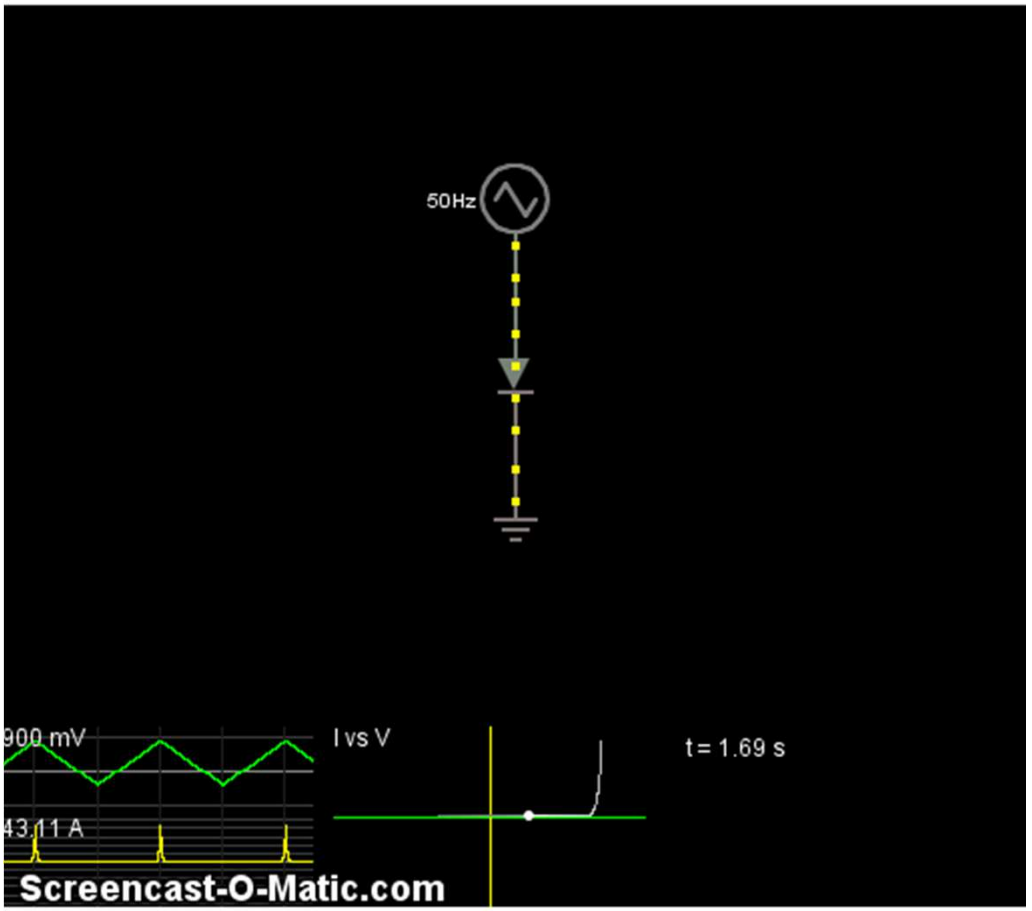


Fig 1: Setup for Assignment 3

If one leg of the signal is GND,
No current across R_{ref} !

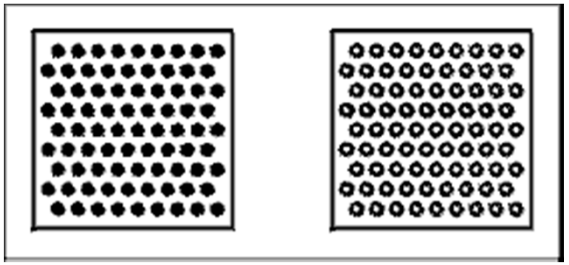
Lab 3: I-V characteristics

http://www.falstad.com/circuit/e-diodecurve.html

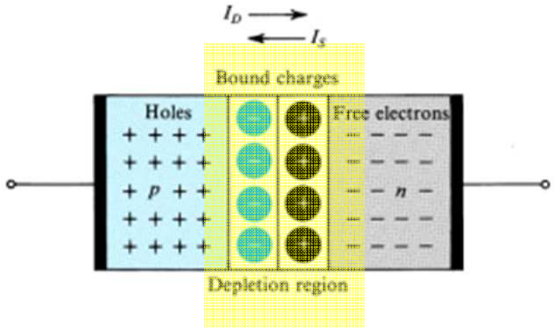


Diode I-V at low frequency

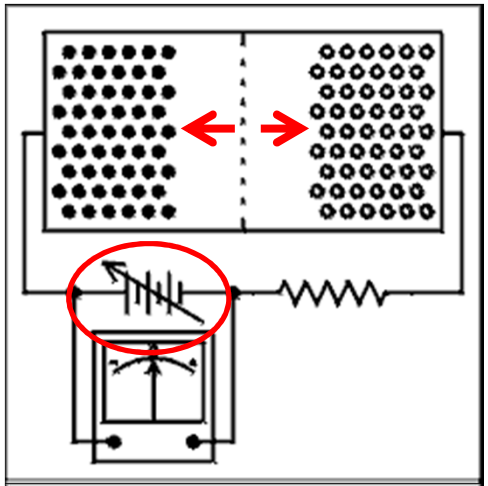
PN junction



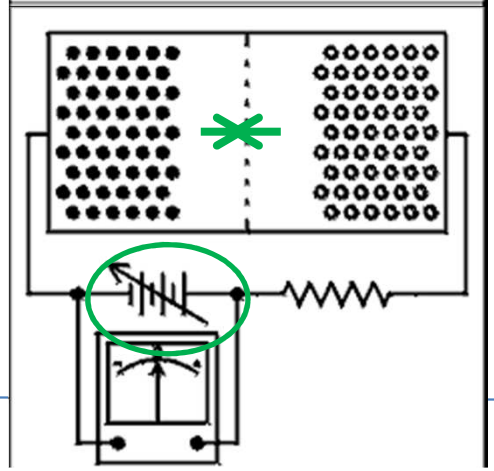
Bound charge between metal electrodes
→ Capacitor



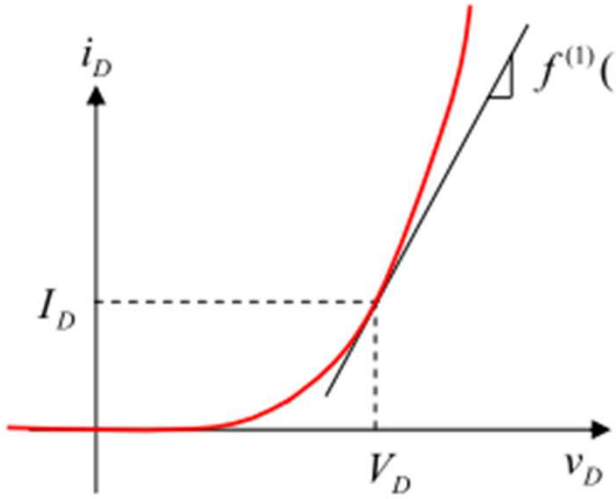
Reverse Bias



Forward Bias



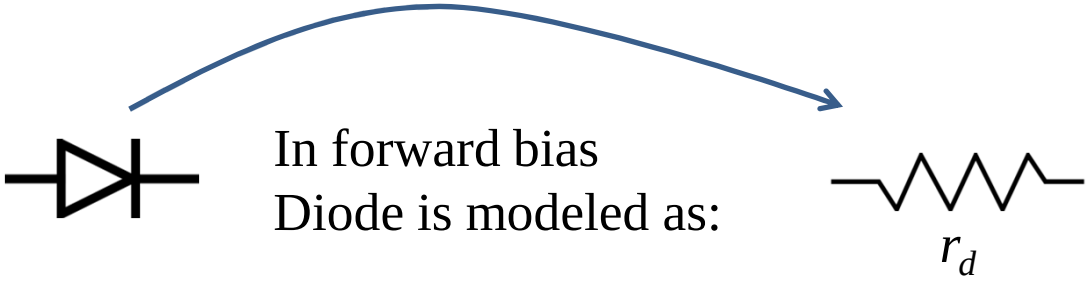
Diode I-V at low frequency



$$r_D \approx \frac{nV_T}{I_D}$$

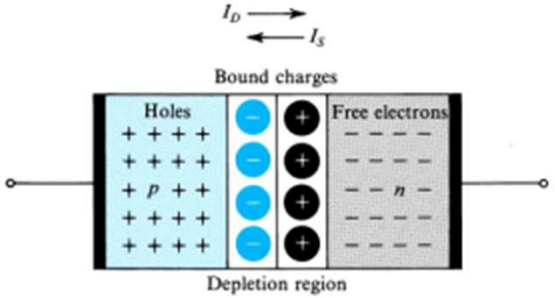
n=2;

V_T = 25mV thermal voltage



Diode I-V at high frequency

Effective capacitance of the depletion layer becomes important at high frequency

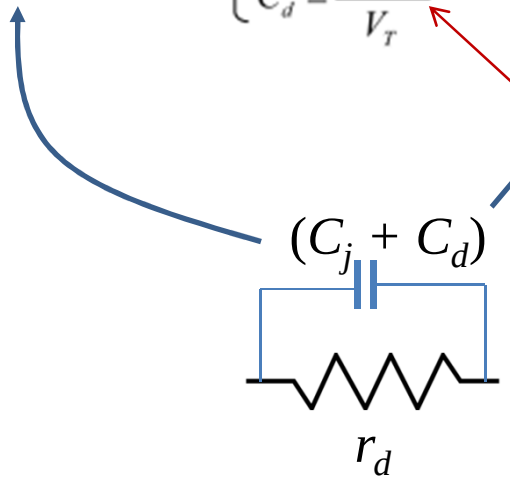


$$r_D \approx \frac{nV_T}{I_D}$$

$$C_d = \frac{\tau_T \cdot I_D}{V_T}$$

Forward bias: $\begin{cases} C_j \approx 2 \cdot C_{j0} \\ C_d = \dfrac{\tau_T \cdot I_D}{V_T} \end{cases}$

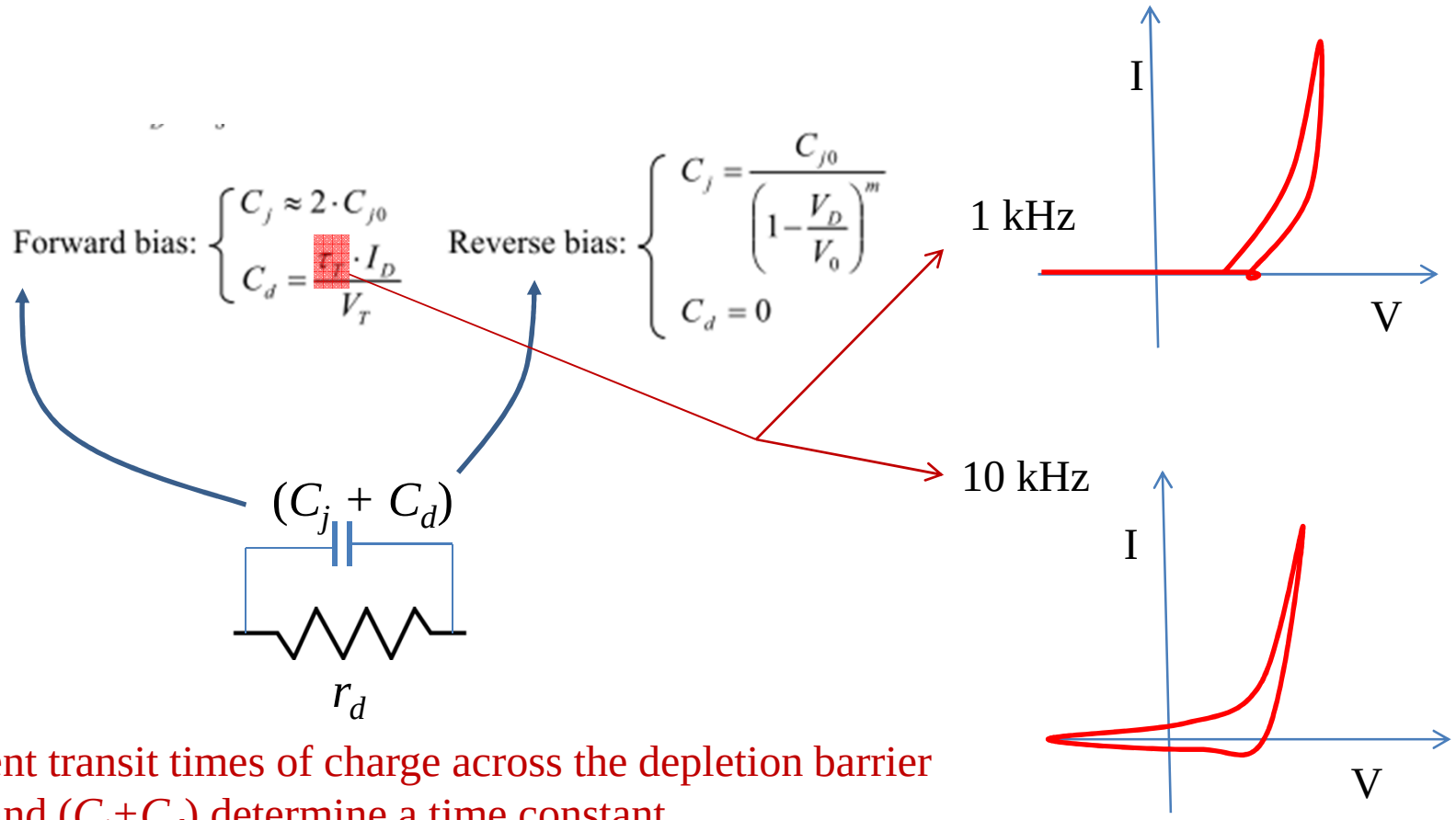
Reverse bias: $\begin{cases} C_j = \dfrac{C_{j0}}{\left(1 - \dfrac{V_D}{V_0}\right)^m} \\ C_d = 0 \end{cases}$



Note:
in dimension:
time * current = charge
So C = Q/V makes sense

Diode I-V at high frequency

Different capacitance in Forward and Reverse bias:

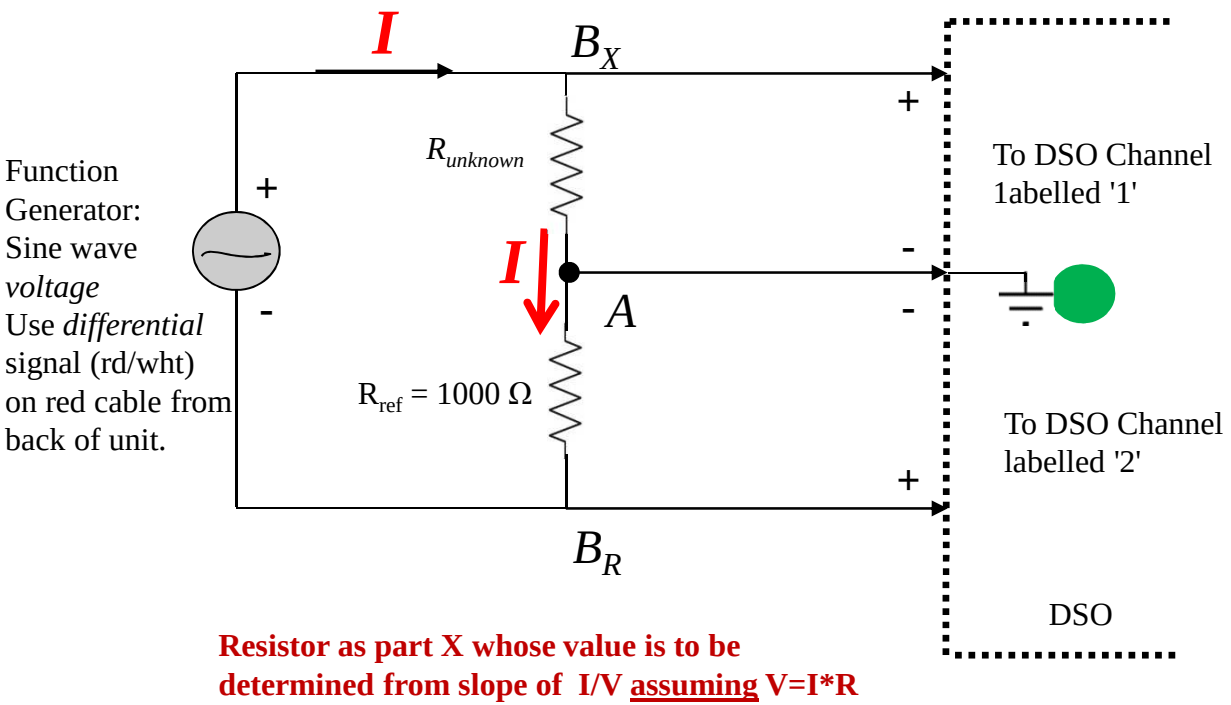


Different transit times of charge across the depletion barrier

→ r_d and $(C_j + C_d)$ determine a time constant

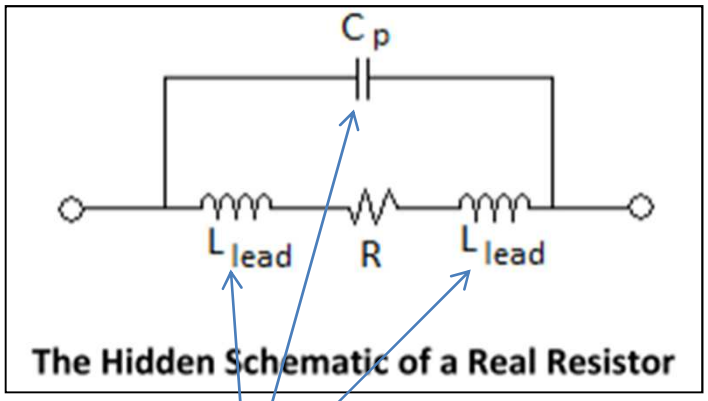
→ As frequency of V_{in} changes, the time constant causes delayed response.

Resistor I-V characteristics

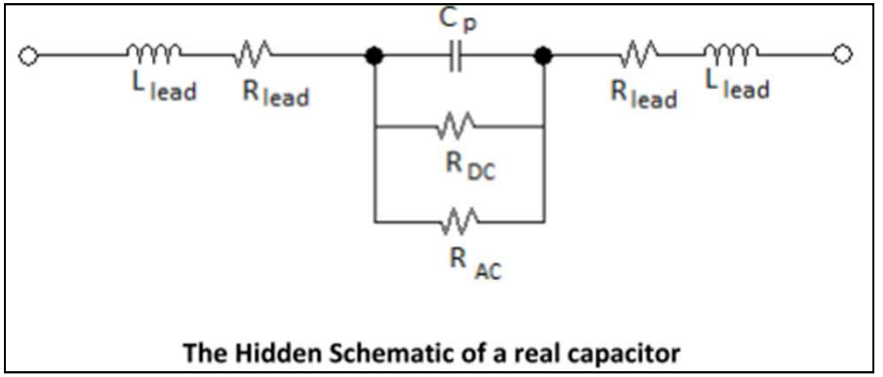


This schematic works fine at low frequency when the resistor behaves like an ‘ideal’ resistor.

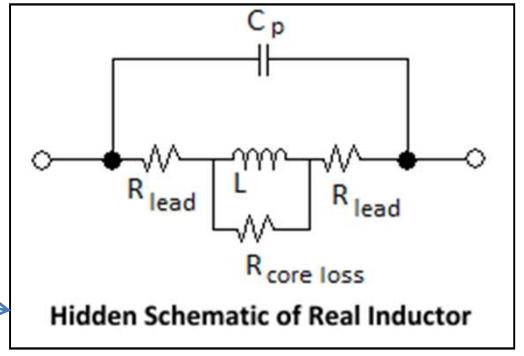
In reality, there is a ‘hidden’ schematic behind every device



The Hidden Schematic of a Real Resistor



The Hidden Schematic of a real capacitor

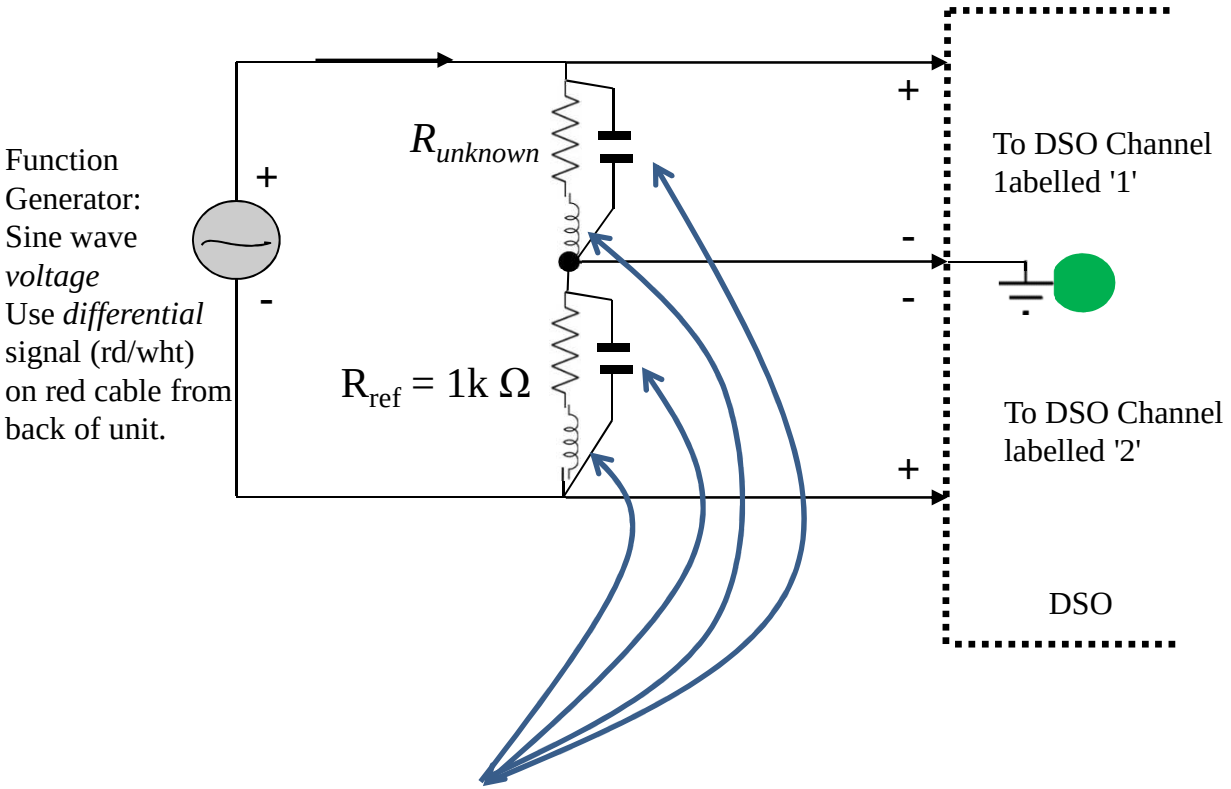


Hidden Schematic of Real Inductor

Note: these are parasitic, frequency dependent effective components of very small value.
So there is no infinite loop here!

See accompanying notes on ‘The Hidden Schematic’

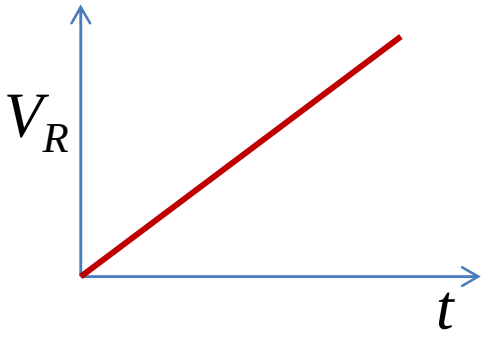
At high frequency, our test setup changes

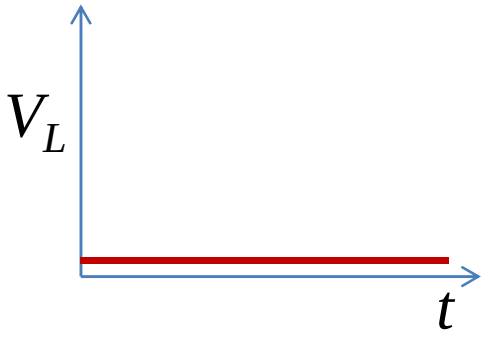


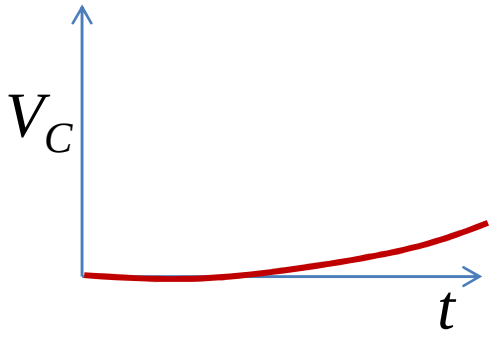
All these parasitic component values are different

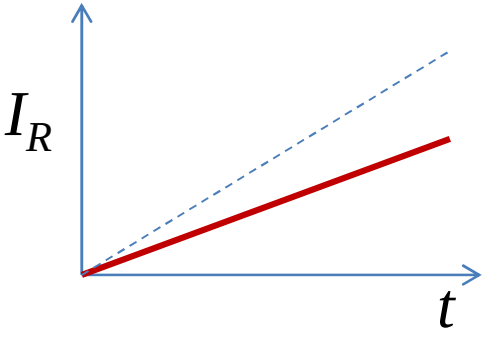
What is the effect of parasitic components on I-V characteristic?

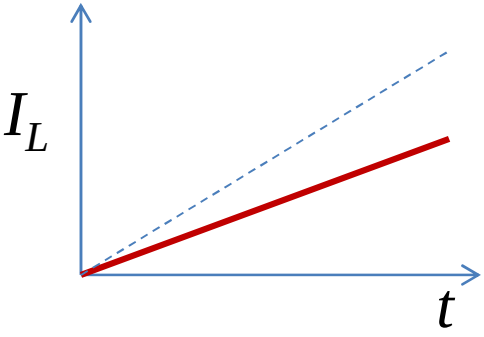
What do V and I look like in the time domain?

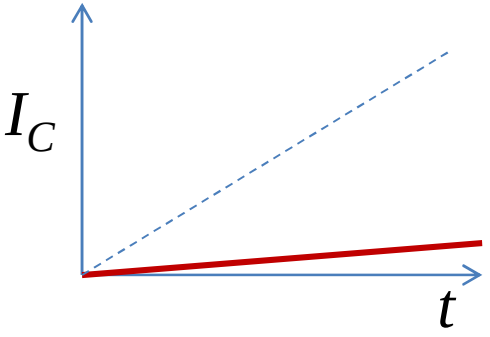












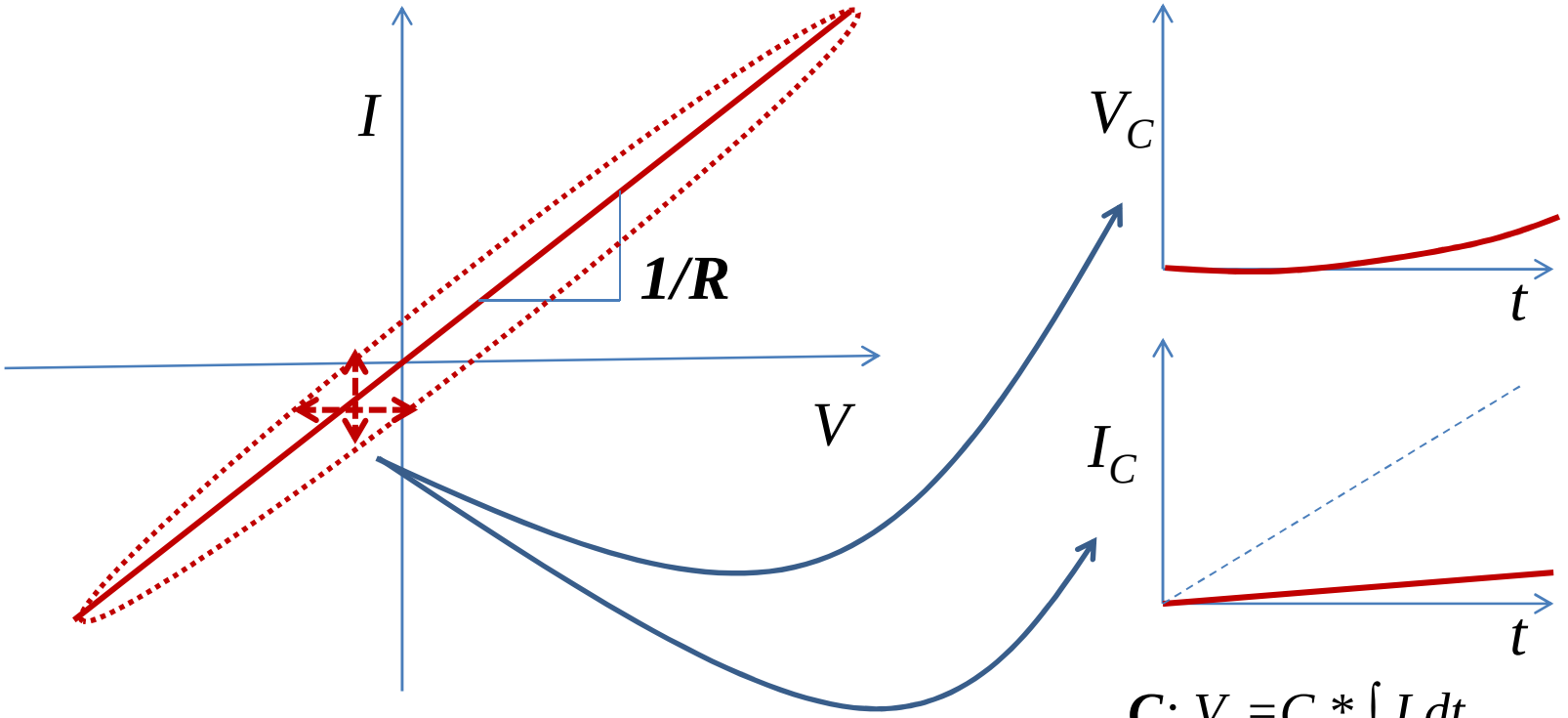
Resistor: $V_R = R * I_R$

L: $V_L = L * dI_L/dt$
Small L is in series, so $I_L = I_R$ *linear*

C: $V_L = C * \int I\, dt$
C in parallel, gets very small I from I_R

What is the effect of parasitic components on I-V characteristic?

In our cool X-Y display format to get I-V characteristics:



Resistor: $V_R = R * I_R$

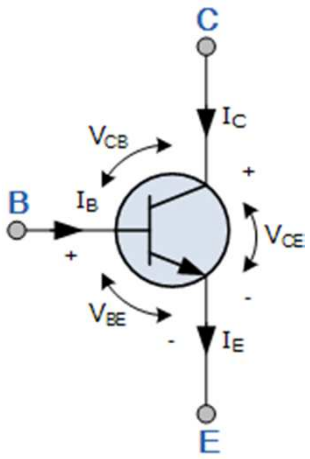
C: $V_L = C * \int I\,dt$
C in parallel, gets very small I from I_R

What's next?

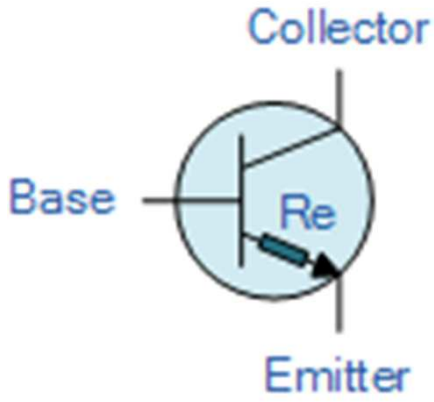
Transistor

Bipolar junction transistor

Graduating from a <u>two</u> terminal device to a <u>three</u> terminal device



NPN transistor



Base-Emitter junction diode highlighted as 'r_e'