**Lab 6 – Bebop to the Boolean Boogie\***

***A:\_\_\_\_/3 B: /4 C: /8 + 5 bonus***

**Goal:**

This lab is split in three parts of increasing difficulty:

1. (Somewhat difficult)  
   We will learn a simple technique to store *n* bits of data into an *n* bit memory given a single serial input line to the memory. We will work with *n=4*
2. (More difficult, though not too much if you have understood Part A)  
   We will use the technique developed in part A to make the numbers ‘dance’ around (hence the title of the assignment) – this can be used to create blinking lights like those used on festive occasions
3. (Very difficult)  
   We will enhance the technique of Part B to a non-trivial level – and demonstrate how to make the numbers dance around in a random manner to create a sequence of 5 bit (pseudo)random numbers

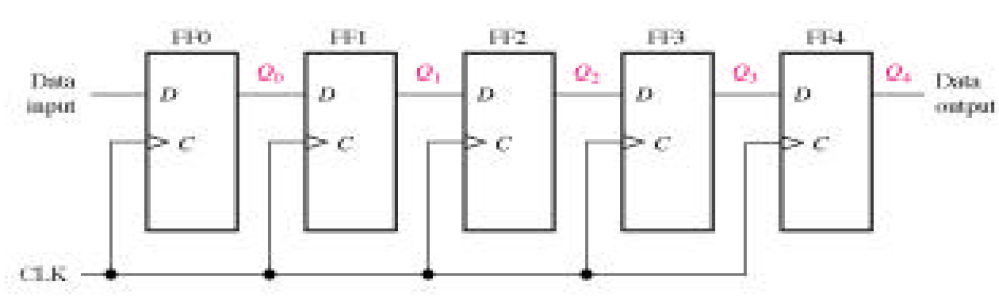
**Part A: Storage of *n* bits**

Recall from earlier exercises that the reliable storage of one data bit requires the use of one D register.

Design a memory circuit that is able to store *n=4* bits of data *D3D2D1D0* with the following constraints:

1. The circuit is driven by a clock signal.
2. The input to your circuit is a *single* serial line. At every clock cycle *i = 0,1,2,3* the values of the data bits *D0­ D1­ D2 D3* (in that order) are made available on the input.

Draw your circuit design here:



Basic 4-bit shift register as shown above

Build your design with the 74LS175 IC. It is useful to connect an LED+220Ω at the output of each D-register to clearly indicate the status of the bit.

Demonstrate its operation by using the 1 Hz clock and sending in a simple input like 10001 (using the push button switch on the logic signal generator). . Note that after the 4th clock input, your memory will start getting overwritten!

**Part A: /3 marks**

*\*Bebop to the Boolean Boogie: An unconventional guide to electronics, ebook by Clive Maxfield*

**Part B: Make *n* bits perform a rhythmic dance**

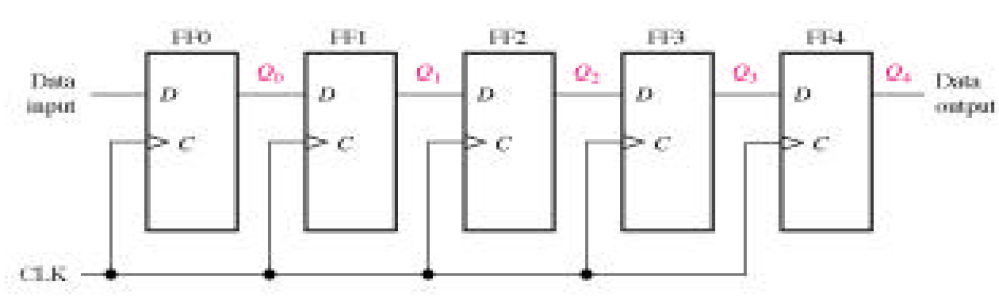
Recall the use of decorative lights in recent festivities – they typically have a string of lights with the on/off states alternating in time to give an illusion of motion along the length of the lights.

Modify your circuit of Part B, to make such a dancing light pattern that repeats itself long as the clock signal is sent in.

*Hints:*

1. ‘Repetition’ usually equates to some type of feedback
2. Each D register has both a Q and Q-bar output
3. You can do this by just re-arranging one of the inputs & outputs in the memory stages.
4. Only one extra connection is needed over the design of Part A
5. You will need to choose a suitable state *D3D2D1D0* to be stored.

Draw the (re)-design of your circuit here. Modify the connections of Part A on the breadboard to demonstrate its operation



Q

Q

Q-bar from last D is fed to D of first bit.

After global reset of the D, and sending clock pulses should see

advancing sequence of a fixed pattern … (1110 in the above design) other patterns are possible based on choice of Q/Qbar taps

B: /4

C: /3 : Basic design

/5 : Choice of DA DB

/5 : Proof of randomness

**Part C: Make *n* bits dance *randomly***

In Part B, the circuit was setup to repeat the same sequence of bits.

Inserting a *linear* operation in the repetitive loop can *change* the sequence of bits that is repeated. Two such linear operations are A(X-NOR)B or A(XOR)B which are very much like algebraic multiplication: A(X-NOR)B=NOT[A(XOR)B]=1 only for A=B=0 and A=B=1, 0 if A≠B.

1. The objective of Part C is that at every clock cycle the sequence of bits *D3D2D1D0* must be random
2. This can be done by using the original design of Part A, with the concept of repetitive feedback used in Part B.
3. The feedback must be modified by inserting a linear operation in the path. Tap two suitable bits *DA* and *DB* from the 4-bit memory and insert the *DA*(X-NOR)*DB*operation in the feedback path.

Circuit Design for Part C here:

***3 marks***

Note: Initially you can choose by trial and error which points ‘A’ and ‘B’ to tap as *DA* and *DB* from *D4D3D2D1D0* You must demonstrate that the sequence of numbers *D3D2D1D0* on successive clock pulses at least *looks* random i.e. it does not get stuck at some fixed number which repeats forever.

-Demo -

***5 marks***

For those with a mathematical and/or Boolean inclination for BeBop:

Calculate how long a sequence of random numbers *DnDn-1….D0*such a design would go through before repeating itself. (It’s easy to work this out explicitly with *n=3*)

The general formula is quite simple. It leads to the fact that, for example, a 32-bit memory register with a single linear operation in the feedback can create a sequence of 4,294,967,295 random combinations before repeating.

This is a Linear Feedback Shift Register

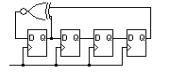
Detailed proof left as exercise to reader.

Useful links:

<http://www.markharvey.info/fpga/lfsr/lfsr.html>

<http://www0.egr.uh.edu/courses/ece/ECE5440/ece5440_LFSR_Counters.pdf>

or Appendix F of the ebook ‘Bebop to the Boolean Boogie’ by Clive Maxfield



***5 marks (and probably a couple of extra pages!)***