

Name: _____

Roll Number: _____

Laboratory 1 -- Introduction to Digital Electronics

This assignment introduces you to the following basic tools and devices:

1. The simplest building block of a digital circuit: the NOT gate
2. You will learn how to read and understand IC datasheets.

Procedure:

The lab is split into two exercises:

1. The first exercise is a theoretical question – answer it and get it examined first.
2. Submit this assignment sheet with your answers to the questions filled in on the spaces provided. Make sure you get all parts of each exercise examined and graded by the TA's during the lab session.

Exercise 1:*(recommended time 30 min)*

Fig 1.1 shows the logic symbol for a NOT gate, with its 'truth table'. For any digital gate, the truth table enumerates all the allowed input conditions and the corresponding output.

The symbols '0' and '1' in the truth table correspond to measured voltages in the circuit.

Typically, TTL gates (Transistor-Transistor-Logic) operate with a $V_{cc}=5V$. A voltage input/output range of 0V – 1.5V corresponds to logic level '0', and 2.5V – 5V corresponds to logic level '1'. These ranges differ slightly for CMOS logic gates.

Compare the two circuits shown in Fig. 1.1a and 1.1b. Convince yourself using simple analog characteristics that both circuits functionally implement the truth table of a NOT gate.

Ignoring the power consumed in the source and a 50Ω load connected to V_{out} , answer the following questions:

Question 1: What is the approximate power consumption of circuit 1.1a when:

- a) The output is in logic 1? _____
- b) The output is in logic 0? _____

Question 2: What is the approximate power consumption of circuit 1.1b when:

- a) The output is in logic 1? _____
- b) The output is in logic 0? _____

Question 3: What is the approximate power consumption of each circuit when it is switching states (1→0 or 0→1)? _Circuit 1.1a:_____ Circuit 1.1b:_____

Hint 1: It is sufficient if you reduce your analysis to the level of 'transistor-as-switch' in digital mode:

For NPN: $V_b \sim 0V \rightarrow$ transistor is 'OFF' and $V_b \sim V_{cc} \rightarrow$ transistor is 'ON' & vice-versa for PNP

Hint 2: A transistor in the 'ON' state can be represented simply as a small effective resistance R_{ON} between the collector and emitter ($R_{ON} \sim R_{BE} = 25mV/I_E \ll M\Omega$). In the 'OFF' state $R_{OFF} \rightarrow M\Omega$.

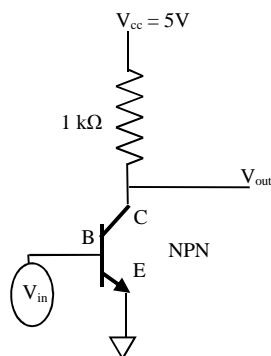


Fig 1.1a : Resistor-Transistor-Logic (RTL)

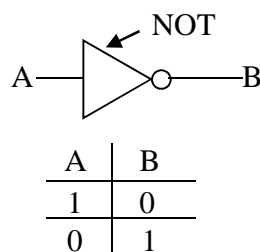


Fig 1.1 NOT Logic symbol and truth table

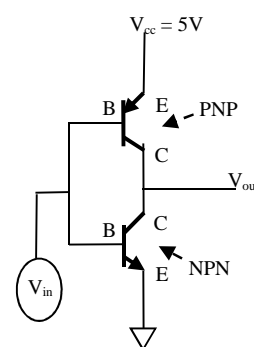


Fig 1.1b : Transistor-Transistor-Logic (TTL)

/2	/2	/2

Ex. 1.1

Ex. 1.2

Ex. 1.3

/4	/1	/1	/3	/15

Ex. 2.A

Ex. 2.B

Ex. 2.C

Ex. 2.D

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Exercise 2: Switching delays in logic gates

(recommended time 1.5 hr)

Introduction: A digital logic gate, like any electronic circuit has a finite switching time. The operating characteristics of logic gates are specified with three important timing parameters:

1. The rise time t_{rise} and fall time t_{fall} of the output signal measured between 10% and 90% of the full-scale values.
2. The propagation delay time t_{PD} is the time it takes the gate to 'calculate and propagate' its logic from its input to its output. This is measured at 50% of the full-scale signal level, i.e. 2.5V in the case of TTL logic. It is approximately the same for both (0→1) and (1→0) transitions.

The timing diagram for a NOT gate in Fig 1.2 illustrates these parameters.

Build the circuit shown in Fig 1.4 using five NOT gates and as little wire as possible.

It's a good idea to use the basic truth table of a NOT gate and a DC input to keep checking your connections as you connect one gate at a time – else it will be hard for you to debug the full circuit!

Questions:

- A) Observe a trace of the signal output from any one of the logic gates, say at point X on an oscilloscope and determine the period of the waveform. From this, infer the value of t_{PD} . Does it agree with the value specified in the IC datasheet? _____
- B) Why have you built the circuit with five gates? What would happen with a different, even number of gates? 4? 6? _____
- C) What would be the advantage of using many more gates (eg 15)? _____
- D) Modify the circuit in Fig 1.2 to have just ONE NOT gate in the loop. Explain the value of the voltage obtained by connecting the output of a NOT gate to its own input in this manner. _____

