Name: *Roll Number:*

Laboratory 8

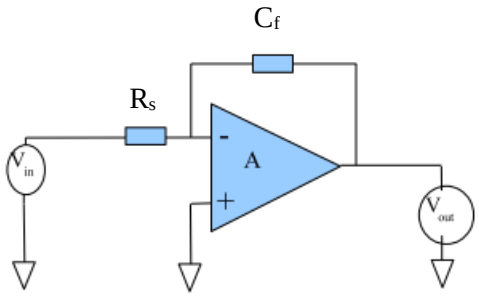
A: /4	**B**: /3	**C**: /3	**D**: /5	**Tot**: /15

Relaxation Oscillators

This lab consists of three modules. We will see how parasitic effects can occasionally be used to a designer's advantage

Part A: Capacitor in feedback loop

Fig 1: C_f in feedback loop.



Consider the circuit of Fig 1. Notice the difference from standard inverting feedback amplifier: the feedback resistor has been replaced by a capacitor C_f.
Consider the mathematics below and choose the *correct* type of capacitor C_f(electrolytic or non-polar)
C must be non-polar polystyrene signal cap

Q1: Calculate the *time-domain* response of $V_{out}$to V_{in}. We have generally calculated the gain of such feedback circuits as $(1+Z_f/Z_s)$ where Z_f and Z_s are the impedances in the feedback and source connections. The time-domain response requires you to apply the golden rules of opamp design *and* the current-voltage relationship for a capacitor $I = C\,{}^{dV}/_{dt}$ followed by some algebra.

Current at (-) input : $V_{in}/R + C\,dV_o/dt = 0$ so $V_o = -1/RC\int V_{in}dt$ → Integrator (with – sign) /1

Q2: Choose suitable values of the passive components R_s ,C_f such that the time constant of your design is 1 ms. /1

Q3: Build the circuit of Fig 1 and drive it with a *square*V_{in} of amplitude 2V peak-to-peak. Draw a diagram of your observations here and verify that your calculations of Q1 above are correct.

Square integration → triangular waveform /1

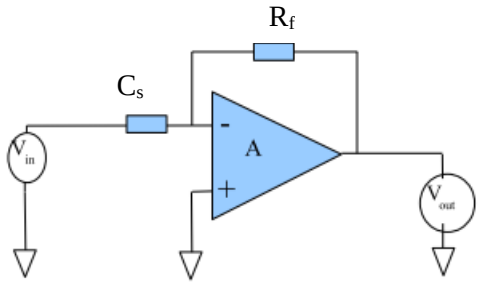
Q4:Set V_{in}=0 by grounding it. Turn off supply to the circuit. When you turn the supply back on, observe the trace of V_{out} on a long time scale ~1 sec on the DSO. Record your observations here, and state a possible hypothesis for the observed behavior

Small internal input offset voltage of opamp (V_{os}) is integrated until the output saturates /1

Name: *Roll Number:*

Part B: Capacitor connected at Input

Fig 2: C_s at source



Consider the circuit of Fig 2. Notice the difference from standard inverting feedback amplifier: the *source* resistor has been replaced by a capacitor C_s.

Q1: Calculate the *time-domain* response of V_{out} to V_{in} as in Part A. The time-domain response requires you to apply the golden rules of opamp design *and* the current-voltage relationship for a capacitor $I = C\,{}^{dV}/_{dt}$ followed by some algebra.

Current at (-) input : $V_o/R + C\,dV_{in}/dt = 0$ so $V_o = -RC dV_{in}/dt$ → Differentiator (with – sign)

/1

Q2: Choose suitable values of the passive components R_s ,C_f such that the time constant of your design is 1 ms.

/1

Q3: Build the circuit of Fig 2 and drive it with a *square*V_{in} of amplitude 2V peak-to-peak. Draw a diagram of your observations here and verify that your calculations of Q1 above are correct.

Square differentiate → flat 0 *except* +/- delta functions at edges

/1

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Part C: Comparator

Recall the simple comparator (with Hysteresis) circuit using positive feedback we studied earlier in Lab 2. The function of a comparatoris to feedback a fraction of V_{out} to the **(+)** input so that when V_{in} exceeds a threshold set by the feedback fraction R_f^+/R^+, the output switches to $-V_{sat}$ and when V_{in} falls below threshold, output switches to $+V_{sat}$

Use your memory/logic and draw the diagram of a simple comparator circuit here, with $V_{in} = 0$

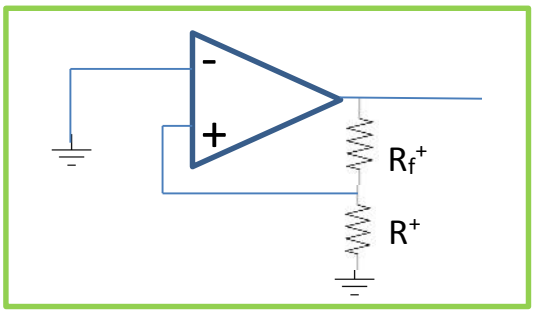

Fig 3: Simple comparator with positive feedback. Set the reference voltage for comparison to $V_{sat} *(R^+/ R_f^+ + R^+)$

/0.25

In view of your measurements in Part A and Part B:

Q1: *Predict* the value of V_{out} in your circuit with V_{in}= 0:

a) What is V_{out} at t=0 immediately when the circuit is turned on? 0V /0.5

b) What is V_{out} in the very short time ~ microseconds after the circuit is turned on? /0.5

c) What is V_{out} in steady state after the circuit has been on for a few seconds: $+/- V_{sat}$ /0.25

Q2: Connect up the circuit you have designed in Fig 3 and *demonstrate* the validity of your predictions

Use this space to record your DSO observations of V_{out} in detail. Note that $V_{in} = 0$ for a), b), c)

/1.5

Part D: Relaxation oscillator

Use your observations and conclusions from Parts A, B and C to make an opamp circuit that demonstrates the following behavior:

1. It's V_{out} oscillates between $+V_{sat}$ and $-V_{sat}$
2. It has no external V_{in} applied
3. The oscillation time period is 1 ms

Hint: You will need to use Part C and any one of Parts A or B

Draw your circuit design here. Calculate and mark the value of the components required.

Comparator with differentiator in negative feedback loop
Relies on delta function created by 0 to $+V_{sat}$ switching to force output to switch to $-V_{sat}$ and vice-versa

/2.5

/2.5

This type of oscillator is called a 'Relaxation Oscillator'. Build your circuit and demonstrate its operation