Reducing AC impedance measurement errors caused by the DC voltage dependence of broadband high-voltage bias-tees

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Abstract—**During the AC impedance characterization of devices, from the kHz-range up to the GHz-range, accuracy can be lost when a DC voltage is applied. Commercial high-voltage broadband bias-tees are often voltage-dependent, which can cause inaccuracies at low frequencies. A calibration technique with applied bias significantly improves the measurement accuracy. Additionally, a bias-tee has been developed with a voltage-independent capacitor, suitable for DC voltages up to 500 V showing excellent performance up to several gigahertz. PIN diode limiters protect the measurement equipment from damage in case of a device breakdown.**

I. Introduction

Wide-band electrical characterization, although preceded by a calibration, could show voltage-dependent measurement errors with or without a device under test (DUT). During the characterization of capacitors, from the kHz-range up to the GHz-range, we found that the measurement accuracy in the MHz frequency range was severely reduced due to an unanticipated DC voltage sensitivity of the bias-tee. Before performing the device measurements with any Vector Network Analyzer (VNA), a calibration is required to subtract the parasitic contributions of the VNA, bias-tee(s), cable(s) and probe(s). A VNA generates AC signals, and can record the magnitude and phase of the reflected and transmitted signals. On each measurement port of the VNA a bias-tee is connected. The function of a three-port bias-tee is to superimpose a DC input voltage with the AC signal of the VNA [3]. Many impedance analyzers have built-in bias networks, but most require external bias-tees for high voltages (typically above 40 V). *High-voltage* wide-band bias-tees are commercially available for frequency ranges from the kHz-range to the GHz-range. These are well suited for many applications such as short pulse measurements. Wide-band measurements are also required for material characterization. We use bias-tees for characterization of capacitors with new dielectric materials.

The DC sensitivity of a commercial bias-tee is shown during the measurements by a gradual change in phase at low frequencies and a resonance. These two effects are systematically analyzed in this work.

In this paper we elaborate how a bias-tee works and we discuss trade-offs made in commercial high-voltage wide-band bias-tee designs. The measurement problems are exemplified through characterization of a commercial Picosecond bias-tee. Furthermore, we mention the properties of ferroelectric capacitors, and we will discuss two techniques to restore the measurement accuracy in the MHz range:

a. through an additional calibration at the applied voltage.
b. a new hardware solution with integrated limiters. The limiters protect the measurement equipment from high-voltage spikes in case the DUT breaks down under DC voltage stress.

We demonstrate the efficiency of these two techniques with two measurement examples: a voltage-independent (NP0) capacitor embedded in a low temperature co-fired ceramic (LTCC) multi-layer board, and a tunable voltage-dependent ferroelectric capacitor with a barium strontium titanate (BST) dielectric [1].

II. Bias-tees in general

Bias-tees are electronic circuits that supply a DC voltage to a DUT, while the AC measurement signal can pass undisturbed from the measurement equipment to the DUT and back. A series capacitor C_s between the AC ports (see Fig. 1) blocks the DC signal from the measurement equipment connected to port 1. A resistor R and/or a coil L provide a DC current and voltage to the device at port 3, while blocking the AC signal from the DC power supply connected to port 2.

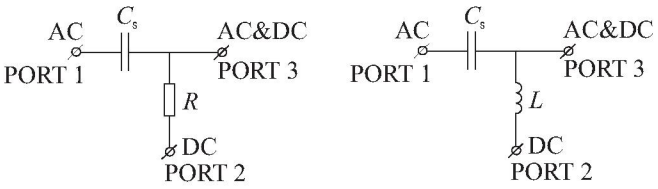

Fig. 1. Simple and common bias-tee designs with a *R-C* or a *L-C* architecture.

The choice for either a resistor or an inductor depends on the amount of DC current required for the application. For relatively small currents a resistor is used, while for relatively large currents (e.g. $I > 10$ mA) inductors are used. Inductors likely become self-resonant at higher frequencies due to parasitic capacitances and require a multi-stage design to suppress those resonances. Resistors can provide a flat impedance over a wide frequency range and are preferred if the small AC dissipation and the DC current limitation can

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be accepted.

Wide-band bias-tees need high value coupling capacitors C_s. The impedance

$$Z_s = R_s + \frac{i}{\omega C_s} \quad (1)$$

should fulfill the relation and the reactance

$$|Z_s| \approx \frac{1}{\omega_c C_s} \lesssim 50\ \Omega \quad (2)$$

at the lower cut-off frequency ω_c. The coupling capacitor will otherwise reflect most of the AC signal. The series resistance R_s models the power dissipation of C_s. It is approximately equal to the resistance of the metallic electrodes and connectors. The capacitors should be small in physical size to avoid parasitic inductances and resonances at high frequencies.

III. Commercial bias-tees

Many commercial high-voltage wide-band bias-tees are built with capacitors with ferroelectric layers, which are much smaller in physical size compared to voltage-independent type NP0 capacitors with the same voltage rating. Albeit, this comes at the expense of a substantial voltage-dependence. The influence of a variable coupling capacitor is strongest at low frequencies when the imaginary part $(\omega C_s)^{-1}$ becomes a significant fraction of the impedance of the DUT. At high frequencies the impedance of a ferroelectric capacitor (see equation 1) is dominated by the series resistance R_s of the metal electrode layers $Z_s \approx R_s$. The voltage-independence of the series resistance of the metal electrodes thus allows a voltage-independent calibration at high frequencies. The next section discusses the properties of ferroelectric capacitors in more detail, including some examples of their use in microwave circuitry.

IV. Ferroelectric capacitor test-structures

We use bias-tees mainly to assess the performance of thin-film ferroelectric capacitors over a wide frequency range. Wide-band measurements are required for material characterization to determine dispersion caused by: leakage current effects, relaxation effects (e.g. in ferroelectric capacitors), distributed effects, electro-acoustic resonances (e.g. SAW [4], or BAW [5]), ferroelectric hysteresis effects [6] or to verify the component specifications. Wide-band bias-tees are most versatile and hence popular components. In ferroelectric capacitors the relative dielectric constant ϵ_r and the loss tangent $\tan\delta$ change due to a saturation of the polarization with voltage (non-linear behavior), a change in the crystal structure with temperature and relaxation of dipoles [7]. In the low kHz frequency range, leakage currents, ferroelectric domain switching, domain wall movements, impurity atom reorientation or space charges dominate the capacitive response. At high frequencies atomic and dipole relaxations and soft phonon modes contribute to a high dielectric constant. Determining the performance in the kHz–MHz frequency range is crucial for obtaining insight into the quality of the dielectric layers. Such tunable ferroelectric capacitors can be integrated in microwave applications such as impedance networks [8], phase shifters [9], or in RF filters [10].

To draw profound conclusions about the performance of the capacitive test structures from kHz–GHz frequency range, the measurement errors caused by a bias-tee with applied DC bias, should preferably be negligible during the characterization. Hence, the measurement errors should be reduced as much as possible.

V. Reducing measurement errors in the MHz frequency range

This sections describes two options two reduce the measurement errors caused by a voltage-dependent commercial bias-tee at low frequencies.

A. An additional open calibration standard

To demonstrate the effect of a voltage stress on the transmission path, the phase of the signal was analyzed. The phase error determines the accuracy of capacitance measurements. In the experiments an Advantest R3767CG VNA was used with external bias-tees. A commercial, very wide-band (f = 20 kHz–18 GHz), high-voltage (max. 200 V) Picosecond 5530A-104 bias-tee [11], suited for low-current applications, was utilized. A two-port measurement setup is used and two Picosecond bias-tees were connected in series, so that the AC ports are connected to the ports of the VNA (see Fig. 2).

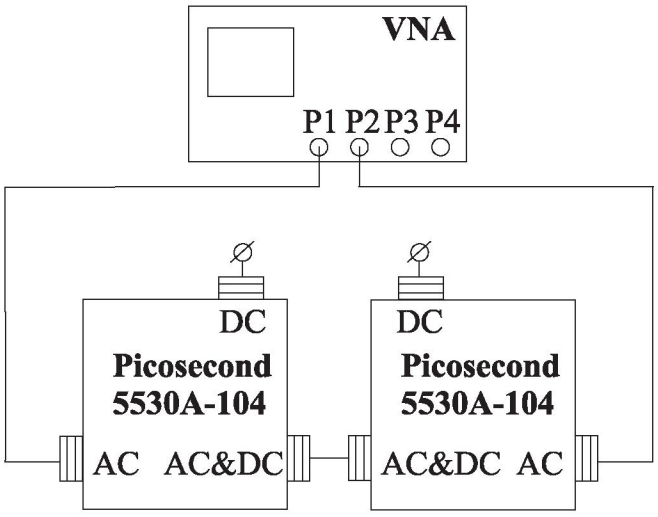

Fig. 2. The RF measurement setup which was used to show the phase difference over frequency before and after applying V_{dc} = 60 V. Two commercial bias-tees Picosecond 5530A-104 were connected in series to port 1 (P1) and 2 (P2) of the VNA. The AC power of the VNA was set at P_{AC} = 0 dBm.

The DC voltage was isolated from the VNA by the blocking capacitor in each bias-tee. The phase of the transmission signal

S_{21} was analyzed. After a short-open-load-through (SOLT) calibration the bias-tees were measured at V_{dc} = 0 V and disconnected. The bias-tees were then terminated with a short or a load, after which a V_{dc} = 60 V voltage-stress was applied on one of the DC voltage ports. Then the bias-tees were connected again to the RF measurement setup and the S-parameters were obtained (without DC voltage). The phase of the transmission S_{21} before the voltage stress was subtracted from the phase after stress and is depicted in Fig. 3. The effect of a DC voltage stress on the bias-tee is evident. The change in phase can be explained by two causes:

1. a remanent change in capacitance C_s integrated in the bias-tee causes the smooth phase increase at low frequencies. Ferroelectric capacitors are non-linear and exhibit hysteresis as mentioned in section IV.
2. a resonance at f = 3 MHz due to an LC resonance or due to an electro-acoustic resonance of the capacitor of the bias-tee.

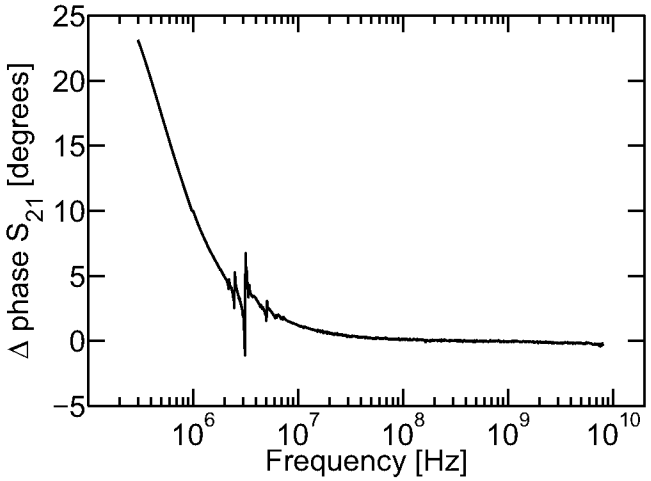

Fig. 3. The difference in phase over frequency before and after applying 60 V DC voltage stress. Two commercial bias-tees Picosecond 5530A-104 were connected in series to two ports of the VNA (see Fig. 2). The AC power of the VNA was set at P_{AC} = 0 dBm.

The phase is critical for a measurement of the equivalent series capacitance C_{ser} of a metal-insulator-metal (MIM) capacitor with a 123 nm thick ferroelectric BST layer (see Fig. 4). A one-port S-parameter measurement was performed on a 30 μm × 30 μm large device electrode from the kHz frequency range up to the low GHz range, using a ground-signal-ground (GSG) probe. A SOLT calibration at V_{dc} = 0 V on a Picoprobe CS-5 calibration substrate preceded the actual measurements. The S-parameters from the VNA were converted to Z-parameters [2] and the R_sC_s series capacitance model of equation 2 was used to extract C_{ser}, which equals C_s. The capacitance shows a typical dispersion at V_{dc} = 0 V (see Fig. 4). At V_{dc} = 5 V an unexpected resonance occurs at f = 3 MHz. The resonances above f = 1 GHz are expected acoustic resonances (BAW's) of the thin film. The measurement results in Fig. 4 demonstrate that the measurement errors with this particular bias-tee were significant close to f = 3 MHz due the voltage-dependent resonance of the ferroelectric capacitor. The effect of a change in the relative dielectric constant of the ferroelectric capacitor DUT with DC voltage is also shown.

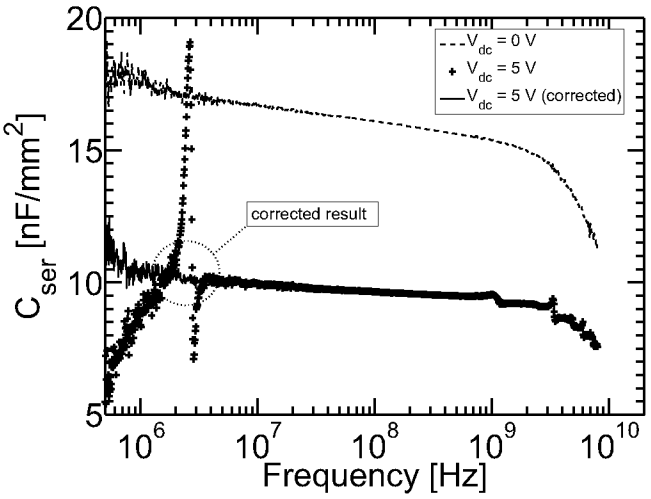

Fig. 4. A wide-band frequency measurement of a series capacitor C_s using an R-C_s model using impedance parameters at room temperature on a 30 μm × 30 μm ferroelectric MIM capacitor with a barium strontium titanate dielectric with a dielectric thickness of d = 123 nm. The solid line shows the resonance can be removed using an extra open calibration at V_{dc} = 5 V.

At low frequencies a capacitive DUT has a high impedance and hence is close to an open-circuit. An open-circuit measurement with a DC voltage before the device measurement can drastically reduce the measurement errors (see Fig. 4). The Y-parameters from the open-circuit measurement at V_{dc} = 5 V were subtracted from the device measurements and the extra error contribution of the voltage-dependency of the bias-tee was successfully removed (see Fig. 4). A short-circuit and a precise 50 Ω load calibration are not possible due to the excessive DC current that would flow. Voltage-independent capacitors as calibration standards would help, but a voltage-independent bias-tee would be better. This solution will be discussed in the following subsection.

B. Hardware solution: development of a new bias-tee

To reduce the measurement errors in the low frequency region, new wide-band high-voltage bias-tees with and without limiters were designed, fabricated and tested. The new hardware solution uses an NP0-type capacitor. The NP0 classification means that the capacitor has virtually no voltage and temperature dependence. For the development of the new bias-tee a *high voltage* 1206 (large) discrete NP0 capacitor with a custom coplanar waveguide design was used with a simple R-C architecture (see Fig. 5).

The bias-tee schematic with built-in limiters is shown in Fig. 6. The limiters were added to protect the VNA from a DC voltage spike when the DUT breaks down during measurement. If no high voltages are required during the measurements the diodes can be omitted to improve

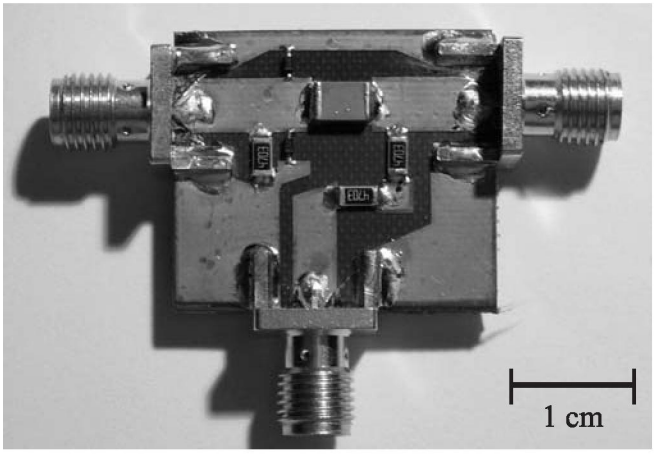

Fig. 5. A top view of the newly developed bias-tee.

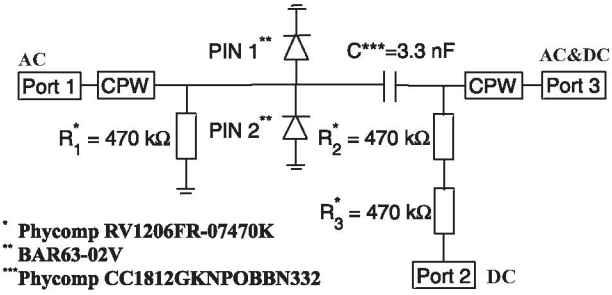

Fig. 6. The schematic of the bias-tee with multiple resistors, a large capacitor, the PIN diodes and the coplanar waveguide matched to 50 Ω at which port 1 = AC signal, port 2 = DC-signal, and port 3 = AC & DC signals.

the transmission path at higher frequencies (this will be exemplified later in Fig. 9). A Taconix RF TLX laminate substrate was used because of its very low loss ($\tan\delta = 0.0022$ at f = 10 GHz), low and stable relative dielectric constant ε_r = 2.45, low moisture absorption (< 0.02%) and thermal and mechanical stability. A patterned copper layer (35 μm thick) covers the upper side of the laminate; the same copper layer forms a continuous ground plane at the backside.

Three-port measurements were performed to characterize the bias-tees. The results of the new bias-tee with diodes were compared with a commercial wide-band high-voltage Picosecond 5530A-104 bias-tee. The return loss S_{11}, the reverse transmission S_{13}, and the isolation loss S_{12} are shown in Fig. 7, Fig. 8, and Fig. 10, respectively. In Fig. 9 the magnitude of the transmission S_{13} of the bias-tee with diodes and the bias-tee without diodes are compared.

The Picosecond bias-tee has a resistor of R = 1 kΩ and a capacitor of C = 82 nF, compared to R = 1 MΩ of the new bias-tee with a C = 3.3 nF. The lower capacitance of the new bias-tee has two reasons: The amount of stored energy that could damage the equipment at the higher voltage rating

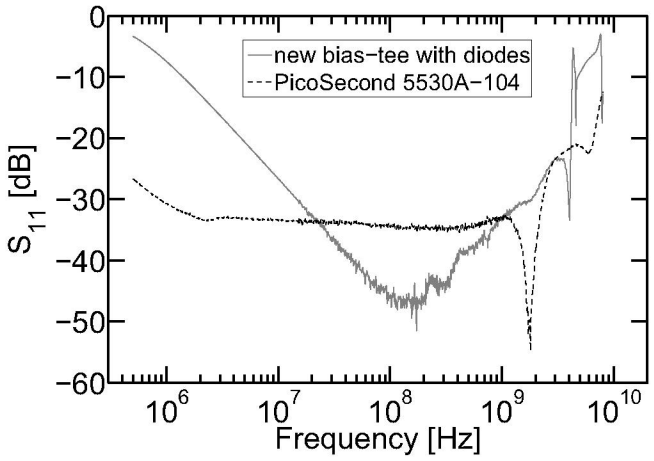

Fig. 7. The return loss S_{11} of the new bias-tee with diodes was compared to the commercial bias-tee at V_{dc} = 0 V with P_{AC} = -10 dBm.

of 500 V is lower, and no high-value surface mount ceramic chip capacitors with NP0 characteristic were obtainable for the given physical size. The new bias-tee has a much higher resistance which results in a lower minimum level of the reflection S_{11} parameter. The capacitance of the new bias-tee, combined with the 50 Ω port resistance explains the high-pass behavior at frequencies below f = 100 MHz (see Fig. 7 and Fig. 8). At higher frequencies the impedance mismatch and parasitic capacitances of the resistors and limiters increase the return loss S_{11}. The -3dB bandwidth extends from f = 500 kHz–3 GHz. Note that the bias-tees without diodes have a wider bandwidth (see Fig. 9).

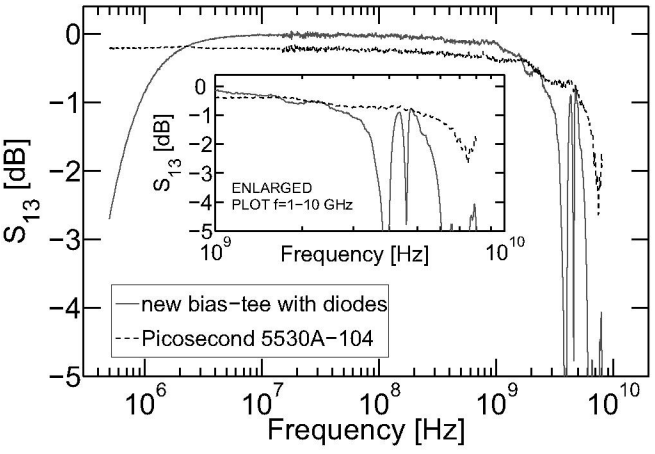

Fig. 8. The reverse transmission path S_{13} of the new bias-tees was compared to the commercial bias-tee at V_{dc} = 0 V with P_{AC} = -10 dBm.

In Fig. 10 the DC bias port isolation S_{12} is shown. The insertion loss S_{12} of the Picosecond bias-tee starts constant due to its 1 kΩ resistance, then followed by a low-pass cut-off. The S_{12} of the new bias-tee in Fig. 10 shows excellent performance up to the resonance around f = 3 GHz. However, the bias-tee can still be used above the resonance

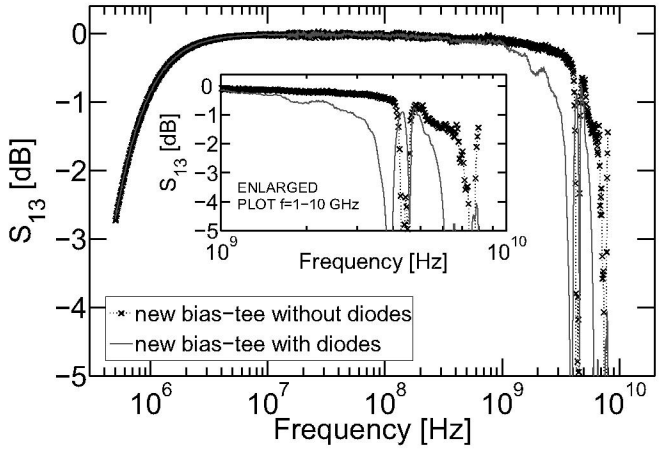

Fig. 9. The reverse transmission path S_{13} of the new bias-tees with and without diodes at V_{dc} = 0 V with P_{AC} = -10 dBm.

when calibrated, but with reduced accuracy. The increase of the S_{12} at f = 10 MHz is due to capacitive coupling to AC ground probably caused by the resistors and diodes.

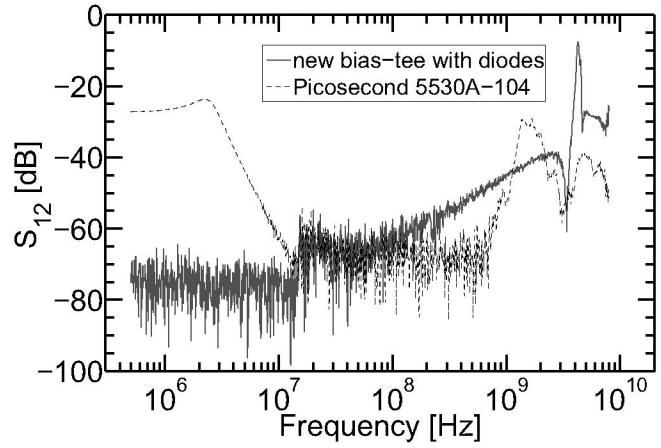

Fig. 10. The DC bias port isolation S_{12} of the new bias-tees using a three-port measurement compared to the commercial bias-tee at V_{dc} = 0 V with P_{AC} = -10 dBm at which port 1 = AC signal, port 2 = DC-signal, and port 3 = AC & DC signal.

A capacitor with an Al_2O_3-based dielectric in a low temperature co-fired ceramic (LTCC) substrate was measured with the new bias-tees at high voltages varying from V_{dc} = 0 to 400 V. The measurement setup is formed by a two-port measurement with one bias-tee on each port is connected to one probe each. The voltage-independent behavior of the bias-tees, with a capacitor test-structure with a value of 8.3 pF is shown in Fig. 11 with respectively V_{dc} = 0 V, 200 V, 400 V, and 0 V once more. The shunt capacitor is calculated from a T-equivalent of the Z-parameters of a transmission measurement.

The newly designed bias-tee showed no voltage-dependent behavior up to 400 volt (see Fig. 11) for the NP0 capacitor embedded in an LTCC substrate. The behavior from f = 100 MHz to 8 GHz is affected by the capacitor connections, but did not result in resonances nor any bias-dependence (not shown).

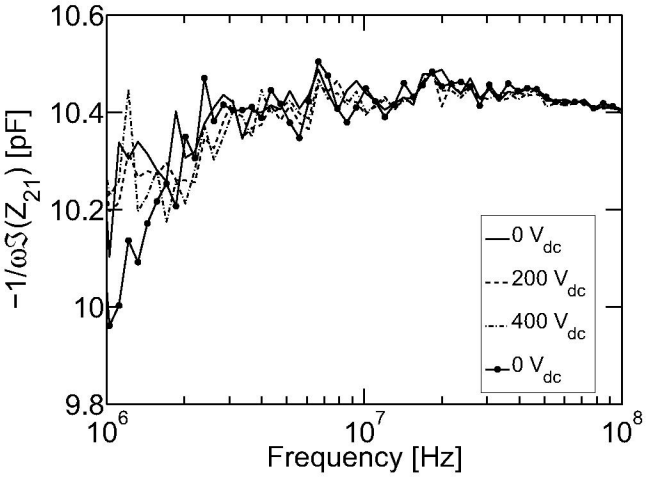

Fig. 11. The NPO capacitance is determined using impedance parameters on an LTCC substrate with an Al_2O_3-based dielectric and is measured at room temperature. The plot shows that a change in DC voltage hardly influences the approximated capacitance.

VI. Recommendations

To improve the bias-tee design further we recommend:

- vias from the top to the bottom ground planes of the laminate (on the upper part of the Fig. 6) could help to suppress resonances of the ground planes.
- the resistor at the AC port could be placed on the other side of the signal path to have a more symmetric current flow in the ground planes.
- to protect the overall circuitry from the environment a package must enclose the laminate substrate and the discrete components.

VII. Conclusion

The AC impedance measurement accuracy for device characterization with a commercial bias-tee with applied DC bias at f<10 MHz has been improved. An additional open-circuit calibration with applied DC bias can reduce the measurement errors significantly if the impedance of the DUT $\gg$ 50 Ω. Furthermore, a broadband high-voltage bias-tee with and without PIN diode limiters was designed, fabricated, and tested. The resulting bias-tee showed excellent characterization results up to several gigahertz with no voltage-dependence impact due to the bias-tee.

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