INTRODUCTION

This application note presents guidelines for creating successful PCB layouts for SMPS applications using CamSemi controller ICs. It is relevant to both RDFC (Resonant Discontinuous Forward Converter) and PSS (Primary Side Sensing) products. Topics addressed include:

- General good and bad design practices;
- Achieving low EMI;
- Thermal optimisation
- Design for manufacture

Further information on CamSemi products is available from www.camsemi.com.

RELEVANT STANDARDS

IPC-2221A Generic Standard on PCB Design

IPC-7351A Generic Requirement for Surface Mount Design and Land Pattern Standard

IEC60617 Graphical Symbols for Diagrams

IEC60950-1 IT Equipment Safety Requirements

IEC61000 Electro Magnetic Compatibility (EMC) Emissions and Immunity

GOOD & BAD DESIGN PRACTICES

PCB layout is usually a compromise between conflicting requirements for size, shape, cost and low EMI. However there some simple, good practice guidelines that should be kept in mind:

Good Routing

- Make track widths appropriate to current carried
- Space tracks according to voltage difference between them
- Keep tracks as short as possible. Prioritise critical ones: highest first (high current, high frequency, high voltage)
- Keep thin tracks away from board edge
- Route tracks to centre of a connecting pad

De-Coupling

CamSemi controller IC's are mixed signal and should be treated as analogue IC's during PCB layout. Power supply decoupling capacitors should be placed close to the pin they are connected to, and the routing distance should be as short as possible.

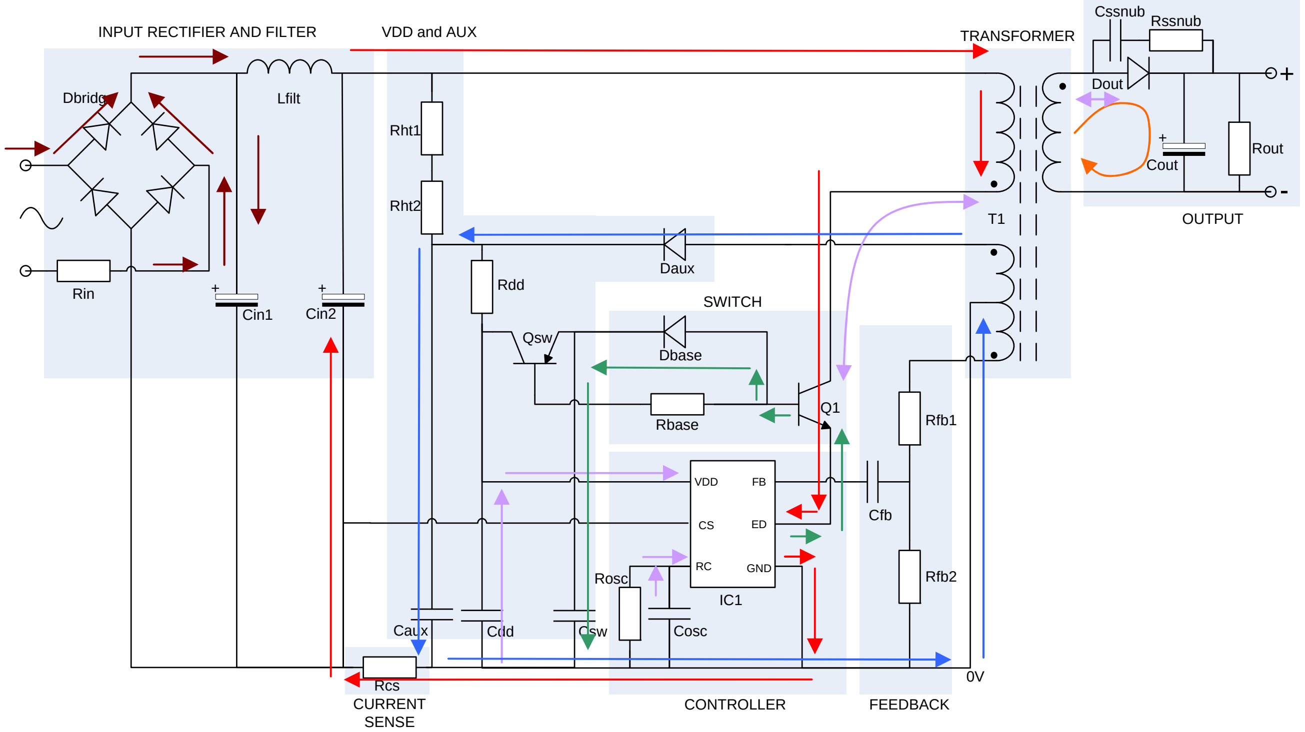

Figure 1: Critical Current Loops in a Typical Primary Side Sensing SMPS Application Circuit

DESIGN FOR EMC

Current Loops in PSS Designs

Current loops (signal paths and ground returns) that carry fast edges are a potential source of radiated EMI. The faster and larger the current fluctuations, the higher the radiated EMI power will be. Also the larger the area enclosed by the loop the higher the level of EMI. The latter is where good PCB design can help, and poor design can cause a real problem. The key is to keep current loops small and run out/return tracks close together. Doing so keeps the loop area and radiated emissions down.

Figure 1 shows the critical current loops in a CamSemi primary side sensing application. A description and example of each loop (as shown by its colour) is given in the next sections.

Red Loop – Primary Current Path

The primary current loop must be kept as small as possible. Figure 2 shows a typical PCB design with the main current path (MCP) indicated with PCB tracking; the main current path is a tight loop.

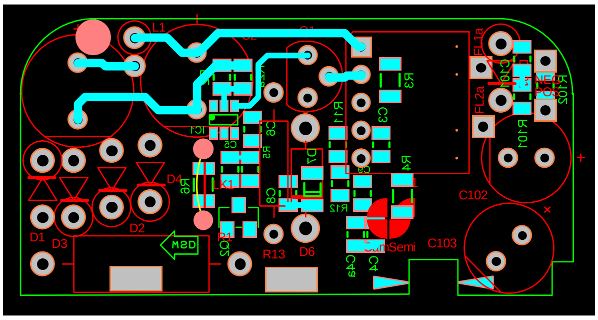

Figure 2: PCB Design with MCP Indicated

Along or near the primary current path, there are connections that need to be kept short. These are:

- From the Q1 collector to the transformer
- From the current sense resistor to the IC

These are described in more detail below.

Current Sense Resistor

The current sense resistor programs the power supply giving it the required rated current. The path from the current sense resistor to the IC is highlighted in Figure 3. The connection should be as small as possible and the track wide (at least 0.02" or 0.5 mm). The current sense resistance is small and any track resistance will affect the operation of the power supply.

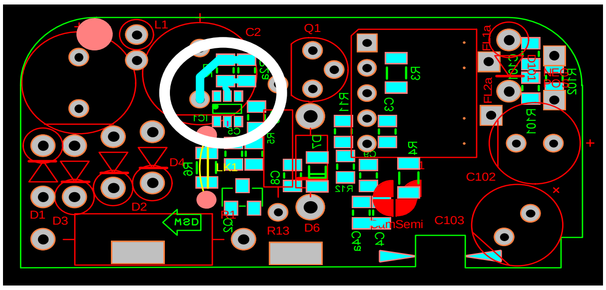

Figure 3: Current Sense Resistors

Q1 Collector Connection

The Q1 collector switches high voltage on and off through the transformer primary winding at a speed of about 50 kHz. This is an EMI source due to the fast edges - with frequencies in the order of 10s of MHz - and fast transients. This connection needs to be routed with the minimum copper area possible to reduce radiated EMI. Figure 4 shows the track highlighted.

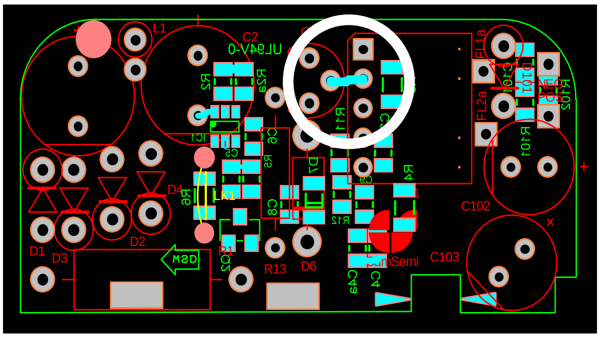

Figure 4: Q1 Collector Path

Green Loop – Emitter / Base Path

The emitter path needs to be kept tight, as a large loop is more likely to cause 'ringing' on the ED pin of the IC. This could result in chip damage or lifetime reduction. Figure 5 shows this path. It is also worth remembering that the majority of this path is part of the main current path.

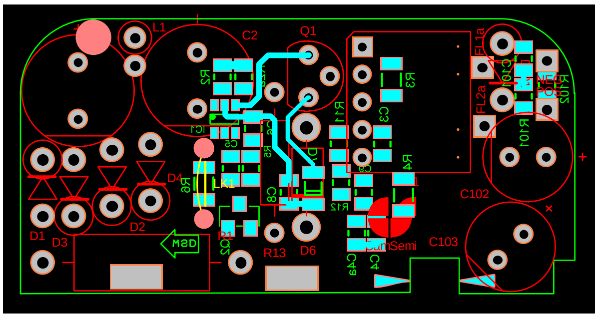

Figure 5: Emitter / Base Path PCB Design

Blue Loop - Auxiliary Decoupling Path

The auxiliary power rail needs tightly decoupled to reduce any EMI resulting from the switching action of Q1. The short auxiliary decoupling path is shown with PCB tracks in Figure 6

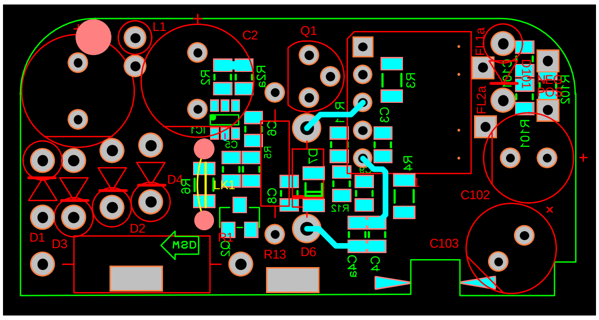

Figure 6: Auxiliary Decoupling Path

Gold Loop - Output Current Path

The output current path is where current from the output diode is smoothed by an output electrolytic capacitor to make a DC output and to reduce EMI. It is important that the path from diode to capacitor is as short as possible, as shown in Figure 7.

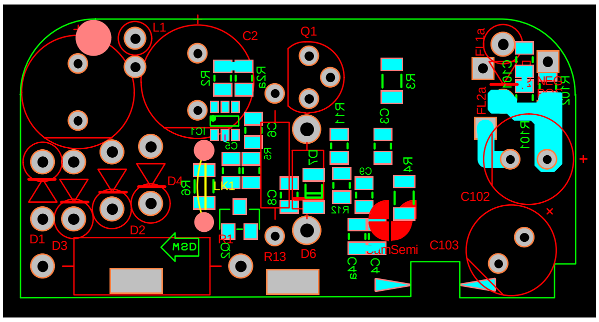

Figure 7: Output Current Path

Brown Loop - Input Bridge Rectifier Loops

There are two input bridge rectifier current loops, depending on which diode pair is conducting. Figure 8 shows a suitable layout.

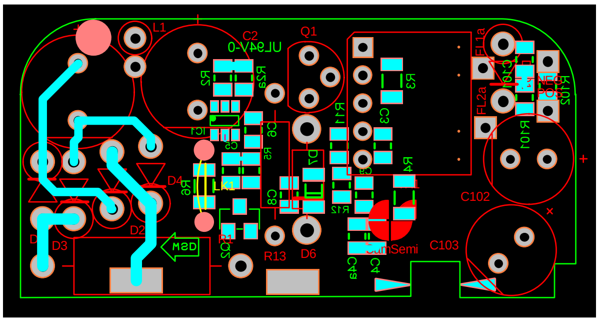

Figure 8: Input Bridge Rectifier Loops

Critical Connections

A number of critical paths should be as short as possible. These are shown in purple in Figure 1 and described below.

VDD Decoupling

The tracks between the VDD and GND pins, and the decoupling capacitor must be as short as possible to avoid poor performance. See Figure 9.

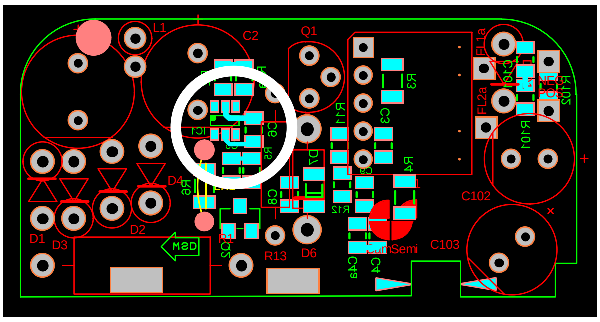

Figure 9: VDD pin Decoupling

Oscillator Path

All high frequency / clock / oscillator tracks need to be kept as small as possible. An example connection is highlighted in Figure 10.

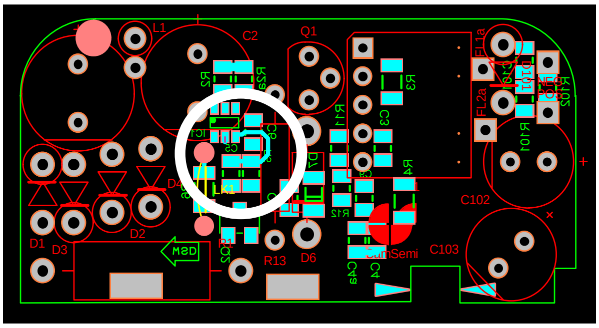

Figure 10: Oscillator Path

Transformer to Output Diode Path

The path from the transformer to the output diode (as shown in Figure 11) needs to be as short as possible, and use the minimum copper area. This connection is an AC voltage, so needs to be short to control radiated EMI.

A compromise is required because a larger copper track or area would help alleviate thermal issues in the output diode. So the copper area needs to be made as large as possible but any unnecessary or oversized features avoided.

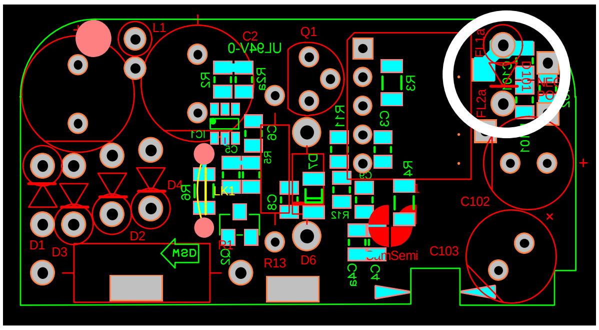

Figure 11: Transformer to Output Diode Path

Output Snubber Components

The output snubber components (Figure 12) should be as close to the output diode as possible to help eliminate EMI from the secondary circuit. NB These components are not always required.

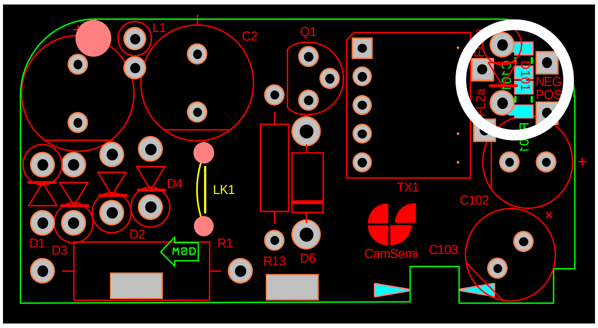

Figure 12: Output Snubber Components

Magnetic Coupling

Magnetic coupling occurs when a wound inductive component is close enough to the transformer to pick up EMI from the magnetic flux of the transformer.

There are two key places where this is a problem:

- Input inductor (Lfilt) - part of the Pi filter
- Any output inductor (if fitted)

This is difficult to fix because most designs are small, so there is limited space available to keep an inductor away from the transformer.

Using components such as electrolytic capacitors as a shield does not help, because any shield used needs to be made from a ferrous material to block the magnetic flux from the transformer.

EMI Control on RDFC Applications

Although PSS and RDFC applications work differently, many of the circuit elements are similar, so the ways of eliminating EMI are similar. The layout guidelines that apply to RDFC are:

- Primary Current Path - Figure 2
- Auxiliary Decoupling - Figure 6
- Output Current Path - Figure 7
- Input Rectifier Loops - Figure 8
- VDD Decoupling - Figure 9
- Q1 Collector Path - Figure 4
- TX to Output Diode Path - Figure 11
- Current Sense Resistors - Figure 3
- Output Snubber Components - Figure 12

Also, bear in mind that magnetic coupling will apply as well.

THERMAL CONSIDERATIONS

Thermal management in enclosed power supplies can be very challenging, particularly in low-cost plug-top adapters. PCBs are generally single sided and do not have much copper to conduct heat away from hot spots. In a sealed plastic enclosure, there is no airflow so poor air circulation. The limited options for dispersing heat from particularly hot components are:

- Use available PCB copper
- Keep components that get hot away from other components

Three components that can get particularly hot are covered in the following sections.

Thermal Control of Switching Transistor

The switching transistor (highlighted red in Figure 13) switches through the primary winding of the transformer. To help keep its temperature down:

- Make pads as large as possible
- Make connections to pads as wide as possible to conduct heat away

These methods have little or no cost penalties. Another way to increase the copper at the transistor is by increasing the copper thickness, but this will carry a cost penalty.

The switching transistor is close to the transformer because of EMC and space requirements, but it is also a source of heat. This means a balance is required between too close for thermal reasons and too far for EMC reasons; Figure 13 shows a layout that strikes a balance between the two.

It is also good practice to have some distance between the switching transistor and the nearest electrolytic bulk capacitor(s).

NOTE: Using a TO92 transistor as the switching device is acceptable for applications up to about 4 W, above this:

- *Use a larger transistor package or*
- *Use a heatsink.*

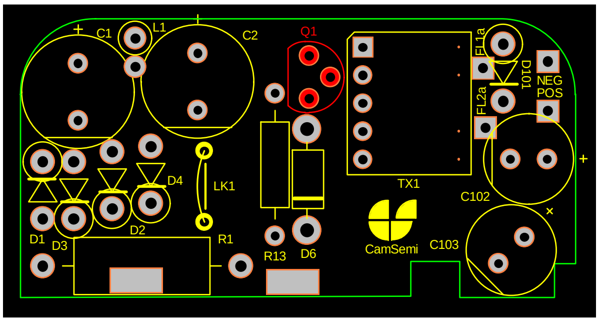

Figure 13: Switching Transistor

Thermal Control of Transformer

The transformer (Figure 14) generates heat because of losses in the windings. When the power supply is operating at full load, the transformer will be running hottest. Because of the relatively large thermal mass and poor thermal transfer to the transformer pins, the PCB design cannot help to alleviate this.

The CamSemi RDFC & PSS design guides have notes on transformer design. Using these guides should help to keep minimise the heating effect.

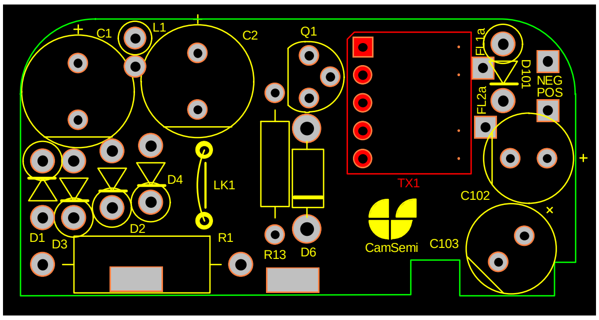

Figure 14: Transformer

The secondary side pins of the transformer are removed to help with creepage and clearance.

Thermal Control of Output Diode

The output diode (Figure 15) can dissipate significant power due to the forward voltage drop and conducted output current, so consider the following when placing the diode.

1. Mounting the diode flat to board: keep copper area of cathode connection to transformer small; make copper area of anode connection as large as possible.
2. Mounting the diode vertically: put diode body on transformer side of connection; keep copper area small; make opposite connection as large as possible in terms of copper area.

Note: Approach 1 is preferred but is not always possible because of space restrictions.

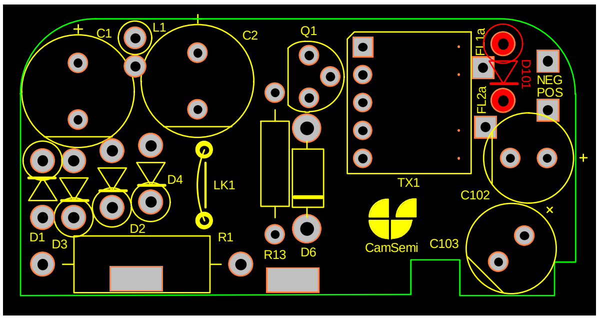

Figure 15: Output Diode

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