Best practice in circuit board design

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Abstract

This paper introduces the basic principals of EM wave propagation within printed circuit board (PCB) structures. Only with a grasp of the basic principals can the design engineer select the most appropriate 'best practice' rules and methods and apply them correctly. The paper demonstrates this principal in evaluating the usefulness of power planes in PCB layout. Having established the paradigm that 'there is no substitute for a first principals understanding' the paper goes on to describe a number of good practice design rules with reference to real world examples.

Introduction

If radio frequency (RF) design is voodoo then 'good' EMC designs must come straight from the paranormal. Not so, the underlying physics is well understood and has been so for over 100 years.

The 'voodoo' perception comes from the way designers, unfamiliar with the physics of what they are doing, apply EMC design rules without any understanding of the whys and wherefores.

The difficulty of calculating the EM performance of a product comes from the complexity of its internal components and physical structures. This usually makes a mathematical model too complex to compute. However this does not present a license to suspend reason and method when designing.

Basic Principals

All best practice rules and methods are based on the physics of EM waves. To select the appropriate method and apply it correctly requires a first principles understanding of EM propagation. A revision of the basic principals will be undertaken here and I will show how this understanding can be used to evaluate and apply the methods that follow.

Waves Guided by Metallic Boundaries

A PCB is a set of copper traces fixed in space by an insulating substrate. Each copper trace is a metallic boundary and when carrying an electrical signal it generates a radiated EM field.

For all metallic boundaries:

> "*If we assume perfectly conducting walls the electric field must be normal to the walls and the magnetic field must be tangential*"[1].

Furthermore the direction of propagation is orthogonal to both.

Remember this basic rule as all that follows is built upon it.

The simplest example is a single copper track (fig 1).

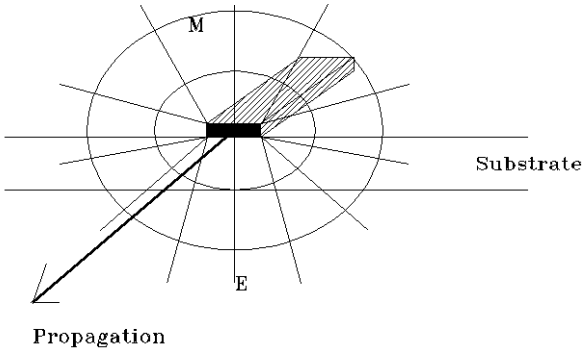

Fig 1 -- Single Track on PCB

A current flowing along the track sets up an electric (E) field, which radiates out from the track in all directions. It leaves the track at right angles to the surface. The magnetic (M) field is constructed by intersecting the E field at right angles at all points.

This represents the worst case EMC scenario as the EM fields radiate out into space ad-infinitum. This track is an antenna. Unfortunately most single and double sided PCB tracks fall into this category.

The situation can be improved by placing a return track (usually ground) to follow the signal track at a constant distance (fig 2).

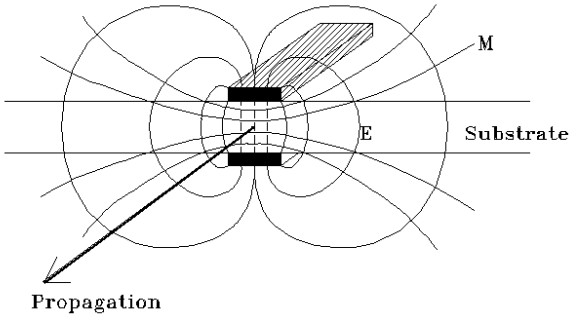

Fig 2 -- Two Parallel Tracks

Much of the E-Field is now confined in the space between the two traces. The confinement of the field is

further improved if the substrate permittivity ε_r is greater than air ε_0 (as is generally the case). In addition if the dimensions and separation of the tracks remains constant a transmission line of constant impedance has been constructed. transmission lines are used to carry fast (high frequency) signals between two points on a PCB.

This form of transmission line is rarely used on PCBs (except accidentally between 2 signal lines to great annoyance). More commonly transmission lines are formed on a PCB with reference to a common ground plane (fig 3).

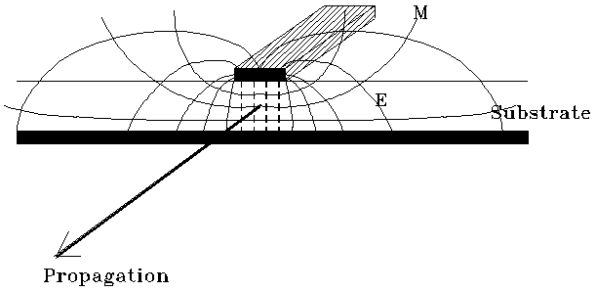

Fig 3 -- Track and Ground Plane

Again most of the E field is confined within the substrate. Additionally there is very little radiation below the ground plane (ideally none). The main reason for using a ground plane is that it allows many transmission lines to be created on one PCB each with a shared return path.

The lines have constant impedance along their length regardless of routing which is a highly desirable property. Note: this is less true at the highest frequencies where abrupt corners in a track also cause reflections. For this reason most PCB designs employ mitred (45°) or chamfered (curved) corners.

The characteristic impedance (Z) of a transmission line depends on its copper thickness, track width, distance from the ground plane and permittivity of the material between track and plane. For the impedance of the line to be constant all these properties must remain constant. If there is an abrupt change in characteristic impedance a mismatch will occur, resulting in a portion of the transmitted signal being reflected back down the line.

Applying a first principals look at the EM fields at the point a track meets a via, shows us instantly that the line characteristics will change abruptly. Therefore vias are a source of reflections particularly if a trace changes layer, as lines on different layers have different Zs due to the difference in separation from the ground plane. For this reason most PCB CAD auto-routers have via minimisation passes.

Finally let's look at the fields associated with a two parallel copper planes as in the example of power and ground planes (fig 4).

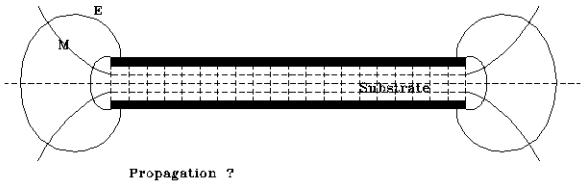

Fig 4 -- Power and Ground Planes

Both E and M fields are regular and confined with aberrations occurring only at the boundary of the planes. For this reason power planes are much beloved of PCB designers but beware we will take a first principals look to see why they rarely live up to expectations!

Power Planes – Myth and Reality

Let's assume power and ground planes are coupled to an IC at a single point source at the via connecting to the power pin (fig 5).

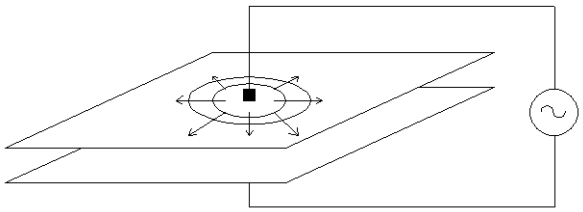

Fig 5 -- EM Propagation from a Point Source

Most digital IC power rails can be modelled as impulse noise sources. Short current pulses (impulses) are generated when digital outputs change state, due to the totem pole (push-pull) drivers used. For a brief period during switching both transistors are 'on' causing a large current drain from the supply.

The current spike propagates out across the power and ground planes in all directions. The wave front propagates out in a similar manner to ripples on a pond when a stone is thrown in. As the wave front expands the energy in it is being spread over an ever increasing area. Therefore although the parallel planes are acting as a transmission line the transmitted energy is being rapidly dissipated.

Increasing the capacitance of the two plates can further enhance this desirable effect. The easiest way to do this, assuming both plates are as large as they can be is to reduce the distance between them. For this reason power planes are generally placed on the inner layers of a multi-layer PCB.

So far all bodes well for power and ground planes but let's look at a practical example (fig 6).

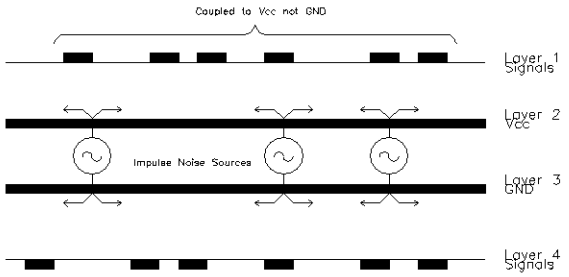

Fig 6 -- 4 Layer PCB Example

Our power planes (inner layers) are now coupled to many impulse sources namely the Vcc pins of various ICs distributed around our PCB.

At any given point on the power or ground plane we will see an instantaneous voltage being the sum of all the wave-fronts incident at that point. The capacitive effect of the two plates will not absorb these voltages entirely because the 'capacitor' is really a transmission line[2] albeit one with a low-Z. For most real-life PCBs this means the power planes are far from quiet. It gets worst; the EM fields associated with the layer 1 tracks aren't coupled to ground at all, they are in-fact coupled to Vcc. Furthermore the E field set up between the plates extends beyond their edges into the dielectric material of the PCB. External decoupling capacitors don't exhibit this phenomenon as their dielectrics are not directly coupled to the PCB dielectric nor are they physically in the same plane.

The other desirable side effect of the power plane, namely its 'free' de-coupling capacitance bears closer investigation. Calculating the capacitance thus:

$C = \varepsilon_0 \varepsilon_r A / d$

$\varepsilon_0 = 8.85 \times 10^{-12}\ FM^{-1}$, $\varepsilon_r \approx 4$ (fibre glass)
$A = 1\ inch^2 = 6.452 \times 10^{-4}\ M^2$
$d \approx 3.5 \times 10^{-4}$ M (4 layer board, 1.6mm thick)

Yields: $C = 65pF / inch^2$

Not exactly a huge capacitance for a whole square inch of copper! For PTFE substrates commonly used with high speed circuits this falls to approx. $40pF / inch^2$.

For these reasons I rarely use power planes preferring to use power tracks and distributed capacitors associated with each individual power pin. Nevertheless they can be used where other signal routing is kept out of the way (fig 7).

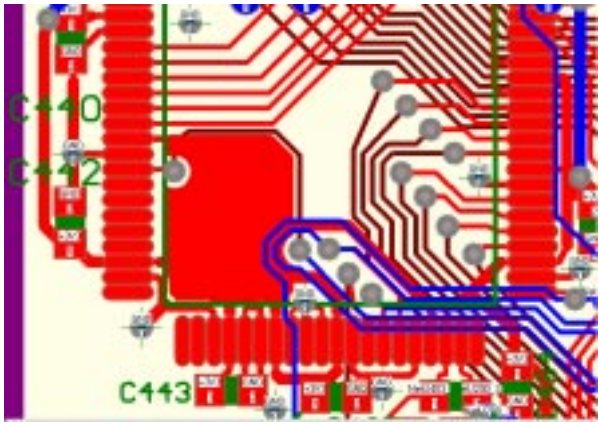

Fig 7 – Power Plane Example

In this example a top copper fill is connected to the 3.3V supply to aid the HF decoupling of a number of supply pins. Ultimately C442 and C443 locally de-couple the supply. The copper fill adds a distributed capacitance of about 3.5 pF, which will only prove useful when GHz frequency components are present. It improves the coupling between the pins, being less inductive that routed copper tracks.

Circuit Partitioning

Best practice dictates considering EMC issues at every stage of the design process. The first consideration, at the first circuit design stage is partitioning.

Circuits are generally designed in blocks. Usually before a circuit for a new product is designed a block diagram of its component circuits is drawn. Blocks are usually functional sub-units. From an EMC perspective we want to partition a product into blocks with different EMC criterion:

- 'Dirty' circuits (that generate EMI)
- 'Clean' circuits (that need protecting from EMI)
- Passive circuits (that are indifferent to EMI)
- Interface circuits that carry EM signals to and from the outside world.

For our purposes the outside world is that external to our product or PCB. Dirty circuits are usually digital and clean circuits analogue. Switched mode PSUs are also dirty circuits. Analogue circuits may also be passive and determining which nodes of an analogue circuit will be sensitive to EMI is not always straightforward. For example op-amps and power-regulators are often susceptible to RF disturbance well in excess of their operational frequency limit[3].

Once we have partitioned our circuit we can then determine what (if any) action is to be taken to ensure the compliance of our product.

For example: with dirty circuits we can either clean them up or isolate them, or some combination of both. Clean

circuits need to be isolated from sources of EMI but may also need their EMI sensitivity 'de-tuning'. We may choose to move passive circuits from our main PCB to a cheaper single or double sided PCB. Interface circuits will need attention to isolate them from the rest of the product and provide protection for ESD and other phenomenon.

The EMI Barrier

Having partitioned our circuit we now want to create partitions on the PCB putting EMI barriers between blocks (fig 8).

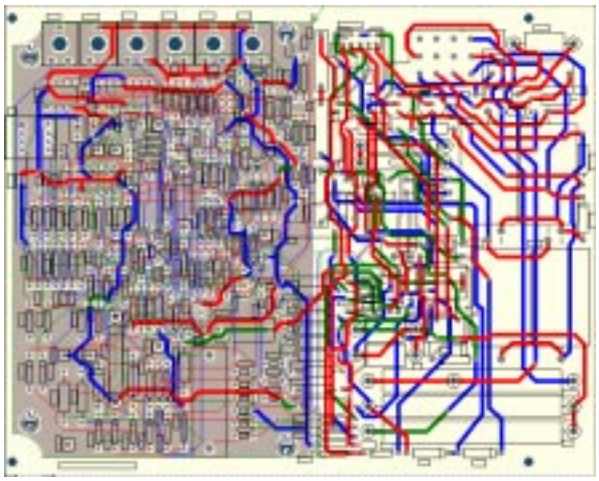

Fig 8 – PCB Partitioning Example

The example PCB has a 'clean' left block comprising of mostly analogue op-amp circuitry with some highly susceptible nodes[3]. It has been laid out using a ground plane (grey) and minimum distance track routing. The right block is a passive I/O block. Signals and power enter by a two connectors (top centre right). Being passive the block did not require a ground plane and so that layer has been reused for tracking.

An EMI barrier was created at the point that the signals from the right block enter /leave the left block. Filtering components were added to each signal and power line. These can clearly be seen in a column (bottom centre). These in-line resistors and inductors have a 'foot in both camps'. Additionally each line is de-coupled by a capacitor to the ground plane at the point it enters the 'clean' block.

This product was housed in an enclosure that was not allowed to be earthed and so a folded sheet steel screening can was designed. You can see the 4 mounting holes marked 0v by which it is bonded to the PCB ground plane. The example shows the successful re-design of a PCB that took the product containing it from an immunity failure at 3 V/M to a pass at 20 V/M.

Splitting the Ground Plane

Figure 8 is unusual in that the 'dirty' block has no ground plane. More usually all the blocks on a PCB have ground planes. The question then is whether or not to split the ground plane at the EMI barrier between blocks.

Splits in ground planes continue to be a contentious issue[4] and whereas once upon a time I always split a ground plane at a barrier I now only do so if there is a compelling reason to. One such reason being the confinement of current spikes and surges to a given area of a PCB. I have even stopped separating digital and analogue ground planes in mixed mode designs and have yet to notice any detrimental affects.

If blocks must have separate planes then ensure that there is a single point of contact between the two which may be either a direct track or a capacitor in the case where ground may have a different DC potential.

When routing tracks on a partitioned PCB place 'keep out' tracks down each boundary to prevent tracks in one block being routed over the ground plane of another. This is essential good practice whether or not a ground plane is split.

Some signal and power lines will inevitably have to cross from one block to another. I always try to put a filter on any such line. For high impedance signals I use an RC filter otherwise an LC filter. Sometimes existing components in a design can be reused to form part of the barrier filter[3].

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Fig 9 – Barrier Π-Filter Example

The layout of a barrier filter is important (fig 9). The eight Π-filters can be clearly seen crossing from the I/O block (bottom) to the digital block (top). Π-filters have been chosen because they are symmetrical, attenuating equally signals travelling in either direction. Axial leaded inductors (10uH) have been used because they have a greater parasitic inductance at the self-resonant frequency and above. SM Chip inductors become capacitors above the self-resonant frequency and have very low impedance at GHz frequencies because of this. 0603 SM capacitors (330pF) have been used to de-couple to the ground planes of each block. These have excellent high-frequency performance due to their small size and chip construction. The capacitors are tucked in under the inductors as a space saving measure.

Think 3D

When designing partitions, barriers or whatever always think of the whole product. PCBs are essentially designed in 2 dimensions whereas the world is 3D. Wiring looms, connectors, enclosure components and other PCBs may well intrude in the near space just above or below a well designed PCB undoing all the good EMC work executed on a board.

Generally keep components (other than barrier filters) away from the boundary between blocks and pay special attention to large components which may be acting as antenna.

Magnetic components, particularly inductors, create M fields that radiate for a considerable distance. They are also susceptible to pick up fields and convert them back into electrical signals. To prevent undesirable effects specify magnetically shielded inductors (rather than those wound on an open former) where magnetic interference is likely to be a problem. Magnetic coupling is a real annoyance in UHF communications products where air cored inductors are used as filter components. A designer will spend time in the trial and error positioning of coils on a PCB and then find (as I have) that the performance of a filter disappears when a PCB has to be re-laid for whatever reason.

Placement and Routing

When the components have all been placed on the PCB the question is which tracks to route first. Before we look at this there are three important points to remember:

- Place components manually. Auto-placers are notoriously indifferent to EMC concerns.
- Place components sensibly. So that tracks can be kept short where they need to be short.
- Be prepared to re-place components during the routing process.

Routing Priority

First I route tracks from IC power pins to their associated de-coupling capacitors. These have to be short direct stubs and de-coupling capacitors need to be close to the pins they de-couple.

Secondly I route high speed clocks and busses. Some PCB packages have a neat feature for routing busses. The operator routes the first bus line manually and the machine fills in the remainder using a close parallel router. I always route important tracks manually and then lock them down so that they are not ripped up during later auto-route passes.

Finally I route all other tracks.

Via minimisation

Always minimise layer changing vias when laying a track. As we have already seen that each via introduces a discontinuity in a transmission line and is a source of potential reflection problems. Most packages have via minimisation passes but I have found that nothing beats a manual inspection of the routed design.

Distributing Power

Having discouraged the use of power planes it seems only right that I should give a method for power distribution on a ‘good practice’ PCB.

I always use the thinnest rather than the thickest tracks I can. This means that their inductance is greatest. The idea is to create a distribution trace that is progressively filtered by the stray inductance of the power track and the various de-coupling capacitors scattered around the PCB. The routing of the power track is not as important as many make out, provided that long runs of it don’t lie close parallel to sensitive signal tracks. For this reason routing the power tracks is not a high priority.

I never reserve a layer for routing power traces alone. Nevertheless a copper imbalance can occur when one of the inner layers is a ground plane and the other contains only tracks. Always check with your PCB manufacturer first and be prepared to add some dummy ground fills on the other inner layer to restore the copper balance if required.

Progressive filtering can be used to great effect if the noisy circuits are routed on one trace and the clean tracks on another, with the noisiest circuits being at the end of the ‘noisy’ chain and the most sensitive circuits at the end of the ‘clean’ chain. This gives the greatest filtered separation between the circuits that need to be the most separate. Sometimes even progressive filtering of this nature needs a helping hand. Figure 10 gives an example of a PCB inductor being used to separate two power supply chains.

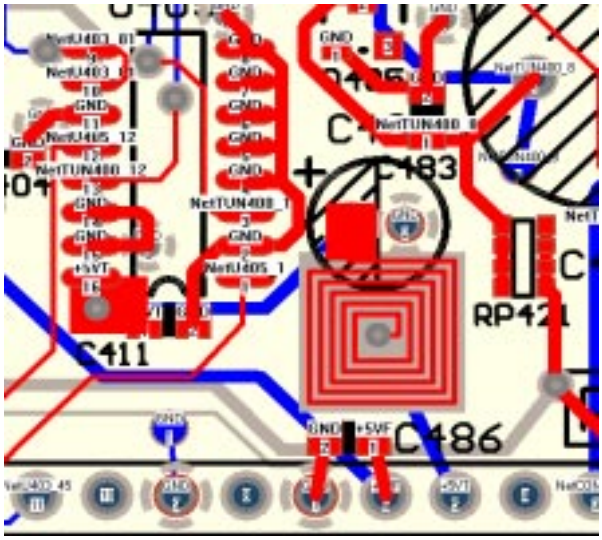

Fig 10 – PCB Inductor Example.

This spiral inductor has a value of approximately 30nH. Notice the square hole cut in the ground plane to accommodate it (ground plane is shown in negative, all other traces positive).

Special ESD Concerns

This paper focuses on the electromagnetic aspects of EMC. There are additional measures that need to be taken when considering ESD (Electro-Static Discharges).

For completeness I will summarise them here:

- Insulation breakdown – If you are designing with components that come into contact with humans be sure that the insulating material doesn't break down at 8kV. This can be a particular problem with thin membranes such as those used in membrane keypads and display diffusers.

- If ESD discharges do get conducted into your product ensure they are arrested properly.

The easiest way to arrest discharges is to raise the impedance of the conducting line. For keypads insert a series resistance of 8.2 KΩ or thereabouts. The clamp diodes built into modern ICs will arrest any remaining current. Where this is impractical use capacitive arrestors (NB: high voltage capacitors tend to be physically large) and /or shottky diode clamps.

2 Layer Boards

Some manufacturers still prefer to stay with 2 layer THP boards even though (A) the EMC benefit of a 4 layer board with its unbroken ground plane is obvious and (B) the cost of 4 layer boards is now only 20% to 50% more than 2 layer[4].

The obvious way of creating a good practice 2 layer design is to relegate all the tracking to one side of the board and use the other-side as a continuous ground plane

Another technique I have used is to split the ground plane into rectangular blocks more or less overlapping on alternate sides of the PCB. These 'ground fills' are then bonded together using via stitching either directly (plane to plane) or indirectly via short stub tracks. This creates a 'patchwork' ground plane of sorts with sufficient free space for tracks on both sides of a board. The technique only works with fairly lightly populated boards and is very time consuming to route because the polygon fills have to be constantly adjusted during the routing process in order to fit everything in.

Armstrong[4] recommends stitching at no more than λ/20, with stub lengths no longer than this. This is actually a very good rule for stitching any ground fill to the ground plane on a multi-layer design. λ is the wavelength of the highest significant frequency for the design (assume a frequency of 1 GHz if not know) where

$$f = C / \lambda$$

NB: C (speed of light) will be approx. 60% of free-space velocity for EM radiation propagating through a FR4 dielectric PCB[4].

References

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[2] 'Rethinking the Role of Power and Return Planes' J Curtis, Conformity Vol 4 No 5. May 1999.

[3] 'Improving the RF Immunity of Sensitive Analogue Electronics' T P Jarvis & I R Marriott. EMC Journal. February 1997.

[4] 'PCB design techniques for lowest-cost EMC compliance: part 1' M K Armstrong. Electronics & Communications Engineering Journal Vol 11 No 4. IEE, August 1999.

About The Speaker

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