Fabrication and Characterization of Ohmic Contacts

Project Thesis in Experimental Physics as a Part of the Master Curriculum in Nanoscience

Lukas Greuter*
Quantum Coherence Lab, Zumbühl Group
Departement of Physics, University of Basel
l.greuter@stud.unibas.ch

*Student of the Nanoscience-Curriculum, University of Basel, Switzerland

April - July 2009

Abstract

To study electron transport phenomena at the interface in semiconductor heterostructures, providing electrical contact is essential. In this project Au/Ge/Au/Ge/Pt ohmic contacts to a two-dimensional electron gas (2DEG) embedded in δ-doped $GaAs/AlGaAs$ were fabricated and studied on two different wafers. Resistances were measured at room temperature and at 4K using a dipstick setup. The expected decrease of resistance was not observed for both wafers for low temperatures. The measured resistances of the ohmics showed a dependence on the annealing temperature during the fabrication process. Treating the heterostructure devices with an etching solvent prior to the deposition, was shown to increase the resistance of the contacts. Finally, surface studies with the Atomic Force Microscope (AFM) revealed a difference in roughness for surfaces treated with the etching solvent compared to non-treated surfaces.

Contents

1 Introduction

Semiconductor materials gained huge attention in the 20th century since their special electronic behavior allows the implementation of novel electronic components. Particularly the invention of transistors laid the foundation for microelectronics, which is nowadays indispensable in many electronic equipments used on a daily basis. The high potential of semiconductors in industry was one of the reasons for the increased research interest on that field. Apart from the practical applications resulting from this research, many new interesting physical phenomenas have been discovered in semiconductors.
An interesting system, which arises in semiconductors is the formation of a two-dimensional electron gas (2DEG). A 2DEG is commonly found in metal-oxide-semiconductor field-effect transistors (MOSFETs), where it arises at the semiconductor-oxide interface. This two-dimensional system allowed to study interesting physical phenomenons and lead to the description of the integer and fractional quantum hall effect in the beginning of the eighties [1], [2]. Few years later quantized conductance of quantum point contacts (QPC) defined in a 2DEG was observed using $GaAs/AlGaAs$ heterostructures [3]. Furthermore the ability to electrostatically define quantum dots (often also referred to as artificial atoms) enabled a lot of new possibiltities to study fundamental physics. Especially the proposal to use electron spins confined in quantum dots to implement quantum bits(qubits) has gained a lot of attention in the last few years [4]. Such qubits would allow the realization of a quantum computer that significantly outperforms the computing ability of classical computers.
Nowadays many experiments based on that proposal are carried out in quantum dots that are electrostatically defined in a 2DEG embedded in $GaAs/AlGaAs$ heterostructures [5]. For these kind of experiments providing electrical contact to the 2DEG is essential. These contacts should be stable, easy to fabricate and ideally obey Ohm's law. Such contacts are commonly realized by depositing a certain composition of metals on the surface, which diffuses into the semiconductor during a thermal annealing process. Although intensively research has been carried out in GaAs, there exist no absolute recipe for the fabrication of ohmic contacts in these structures since some steps in the fabrication are still not completely understood. However, there exist only few systematic studies for the optimization of ohmic contacts. In this project the goal was to study Au/Ge/Au/Ge/Pt ohmic contacts to a 2DEG embedded in δ-dopped $GaAs/AlGaAs$ heterostructures. Therefore Au/Ge/Au/Ge/Pt were successively evaporated on two different wafers with a mesa pattern defined by optical lithography. The effect of using different temperatures during the annealing of the ohmic contacts was studied by measuring the resistance at 4K. Furthermore, a new fabrication step was introduced: prior to the evaporation, the samples were pre-etched with a mixture of $H_2SO_4 : H_2O_2 : H_2O$. This processing may lead to lower resistance values since it is thought that the etching generates a surface roughness, which could have a positive effect on the annealing mechanism. In the following, a short theoretical background is provided before the fabrication protocol of ohmic contacts is described in detail. Finally, measured resistances are presented and compared among the different wafers and procedures used for the fabrication.

1.1 Two-dimensional electron gas in GaAs heterostructures

A 2DEG is formed at the interface between two semiconductor materials with different band gaps. This is the case in $GaAs/AlGaAs$ heterostructures, whereby the electrons from the material with the higher band gap ($AlGaAs$) traverse into the material with the lower band gap ($GaAs$) in order to equalize the Fermi energy E_F (fig. 1). Consequently, the bands start to bend, which can be described when solving the Poisson equation [6]:

$$\frac{d^2V}{dz^2} = -\frac{qN}{\epsilon\epsilon_0} \tag{1}$$

Here $V(z)$ describes the potential. The space charge density is given by $\rho = qN$, where N is the number of dopants per m^3. Since positive charge remains on the $AlGaAs$ side the curvature of the conduction band is positive (fig. 1). Conversely, the curvature is negative at the $GaAs$ side due to the presence of negative space charge. The bending of the conduction band can be approximated by a triangular quantum well, in which discrete states are formed. If these states are lower in energy than the Fermi level E_F they are

populated by electrons. At low temperatures only the lowest state is occupied and hence a 2DEG is formed, where the electrons are confined in the growth direction of the heterostructure. The band gap difference between $AlGaAs$ and $GaAs$ strongly depends on the Al content, which can be customized. Often an Al content of approximately 30% ($Al_{0.3}Ga_{0.7}As$) is used. The charge carriers are provided by using a few atomic Si-doping layer referred to as δ-doping. Thereby the electron density in the 2DEG is strongly dependent on the distance to the layer, which is mostly located above the 2DEG in heterostructures. However the δ - doping layer can also be positioned below the 2DEG, in which case it is referred to as an inverted 2DEG. By illuminating the wafer, more charge carriers get excited into the 2DEG and hence increase its density, which is measureable by a decreased resistance through the 2DEG.
The mobility of the electrons achieved in a 2DEG is generally very large ($\sim 33 \times 10^6 cm^2/Vs$ [6]). This is possible since the lattice constants of $AlGaAs$ and $GaAs$ are comparable and therefore the crystal periodicity is not disrupted across the interface. In addition, the ionized Si - donors are separated from the 2DEG and hence decrease the screened Coulomb potential seen by the electrons.

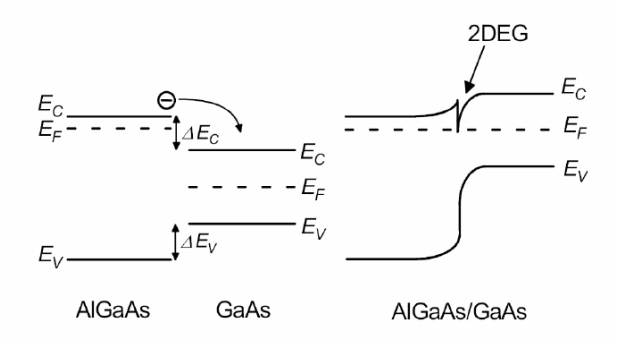


Figure 1: Band-diagram illustrating the formation of the 2DEG. Upon contact of the two layers electrons from $AlGaAs$ layer transverse into the $GaAs$ to equalize the Fermi energy. Consequently, the bands are bent resulting in a quantum well which can be populated forming a 2DEG. E_C (E_V) refers to the energy of the conduction (valence) band and E_F refers to the Fermi energy. Figure adapted from [7].

1.2 Theory of ohmic contacts

1.2.1 Metal-semiconductor interface

To measure the properties of semiconductor devices, the implementation of ohmic contacts is essential. These contacts can be defined as a source of carriers with a non-negligible internal resistance R_C, which obeys Ohm's Law for all density currents of interest [8]. Unfortunately there is no general recipe for ohmic contacts and the ideal fabrication protocol has to be optimized according to the features of the device to be measured.
When implementing ohmic contacts in semiconductor devices, a Schottky barrier is formed at the interface between the metal and the semiconductor (fig. 2). The barrier is described by the band bending which arises due to the balancing of the Fermi levels between the semiconductor and the metal. In this case a potential barrier height ϕ_B emerges from the Fermi level on the metal side to the conduction band of the semiconductor. To move from the metal to the semiconductor, an electron must therefore overcome the energy barrier of $e\phi_B$, which is the difference between the work function of the metal and the work function of the semiconductor. An electron going the other way must traverse over a barrier of eV_{bi}, whereby V_{bi} represents the built-in potential [8].
As seen in figure 2 various electron current components are abundant in a Schottky barrier. j_{1e} and j_{3e} are injection currents and thermodynamically driven, while j_{2e} is the tunneling current. At equilibrium j_{1e} must be equal to j_{3e}(fig. 2a). When a forward bias of V_f is applied (positive voltage to the metal) the Fermi level of the metal will be lowered by $e\,|V_f|$ compared to the Fermi level of the semiconductor and the current j_{1e} is increased by a factor $\exp(e\,|V_f|\,/kT)$ while j_{3e} stays unchanged (fig. 2b). When applying reverse bias to

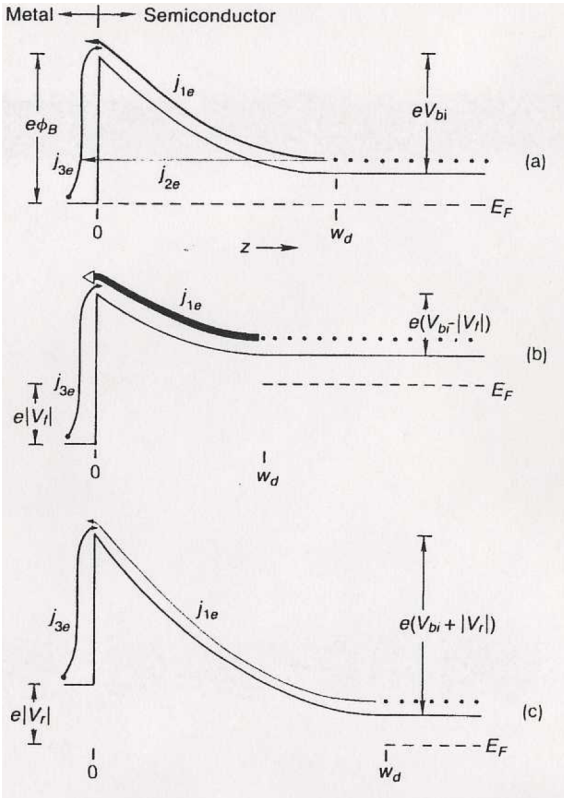


Figure 2: Schottky barrier formed after contact between a metal and a semiconductor. Due to charge balancing, a potential barrier ϕ_B arises. When moving from the metal to the semiconductor the electron needs to overcome the energy barrier $e\phi_B$, while moving the other way an electron must traverse a barrier of eV_{bi}. The current from the metal to the semiconductor(j_{3e}) and vice versa (j_{1e}) are equally at equilibrium because the net current vanishes (a). When applying forward bias (b) or reverse bias (c), the current j_{1e} can be influenced. In this situations the tunneling current j_{2e} can be neglected since the barrier width is too big. Figure adapted from [8].

the metal, its Fermi energy is raised by a factor of eV_f(fig. 2c) and consequently j_{1e} is decreased by a factor of $\exp(e|V_f|/kT)$. Again, j_{3e} remains the same. This situation can be described by the diode equation [8]:

$$j = j_{rs}\left(e^{eV/kT} - 1\right) \tag{2}$$

whereby j is the electron current from the metal to the semiconductor, dependent on the applied voltage V. j_{rs} is the saturation current from the metal to the semiconductor, which is approximately constant for negative V (reverse bias) until breakdown occurs. Since j_{rs} depends on the barrier height ϕ_B equation 2 can be written as:

$$j = K_{rs}e^{-e\phi_B/kT}\left(e^{eV/kT} - 1\right) \tag{3}$$

where K_{rs} is a constant. Apart from very low voltages ($V \ll kT/e$), the situation described by equation 3 does not represent a contact that obeys Ohm's law. Furthermore the current also depends on the factor $\exp(-e\phi_B/kT)$. Since $e\phi_B \gg kT$ for GaAs already at normal temperatures, the current j in equation 3 is mainly limited by the barrier height ϕ_B and clearly not ohmic.
To achieve a high current density ϕ_B has to be decreased by a proper choice of the metal. In GaAs this is not possible due to the large surface state density. Therefore to achieve ohmic behavior the width of the Schottky barrier w_d must be decreased so that the tunneling current plays a central role. The tunneling probability can be estimated by the Wentzel-Kramers-Brillouin (WKB) approximation [6]:

$$T(w_d) = \exp\left[-2\int_{w_d}^{0}\left\{\frac{2m^*}{\hbar^2}V(z)\right\}^{1/2}dz\right] \tag{4}$$

Here $V(z)$ describes the shape of the potential and $V(w_d) = 0$. $V(z)$ is obtained when solving the Poisson equation and with using the depletion depth w_d the integral can be calculated and the tunnel probability becomes:

$$T = \exp\frac{e(V - V_{bi})}{E_0} \tag{5}$$

where $\Delta V = V - V_{bi}$ represents the difference between the external applied voltage V and the bias independent barrier height V_{bi}. E_0 is the energy, dependent on the doping density N:

$$E_0 = \frac{\hbar}{2}\left(\frac{e^2N}{\epsilon\epsilon_0 m^*}\right)^{1/2} \tag{6}$$

Evidently, increasing the doping density decreases the depletion width. Consequently, the tunnel probability increases according to the equations 5 and 6. The situation is described in figure 3. By increasing the doping density, the Fermi energy is lifted closer to the conduction band and the depletion depth is decreased, resulting in a higher tunnel probability. For very high doping densities the barrier gets very narrow and the contact between the metal and the semiconductor can be regarded as an ohmic contact.

1.2.2 Composition of ohmic contacts

Although the 2DEG in *GaAs*-heterostructures is widely used to study different mesoscopic behaviors, there exists no general metallic composition of the ohmic contacts up to now. However the Au/Ge eutectic, which melts at around 360°C is considered to be a permanent feature among the different ohmic contact recipes. Au is thereby assumed to act as the carrier, while Ge is thought to diffuse into the semiconductor to provide the doping, which decreases the tunnel barrier. The used weight ratio of the eutectic is typically 88% : 12%. Additional to the Au/Ge eutectic, Ni was often used as a compound of the contact metal alloys [9],[10]. Thereby the ohmic contacts yield low resistances when the Ni-layer was evaporated as the last layer. The optimal Ni-layer thickness was determined to be approximately one quarter of the total Au/Ge layer thickness. Furthermore, it was shown that evaporation of 107.2 nm of Au, 52.8nm of Ge, followed by 40 nm of Ni gives very reasonable contacts, which were later used for various 2DEG devices [9]. Another study showed

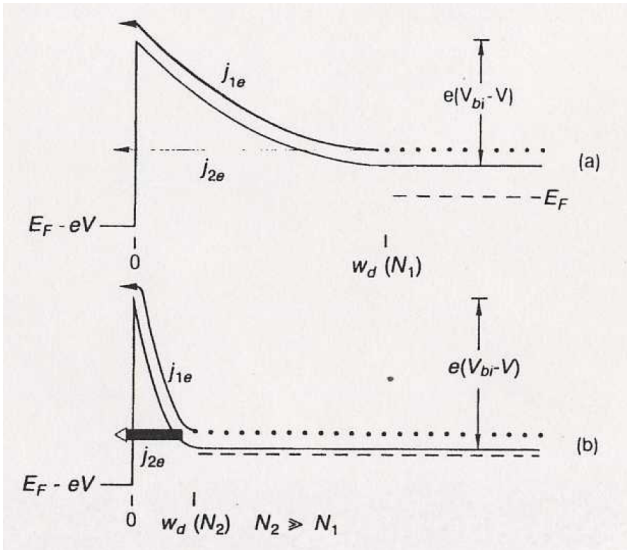


Figure 3: Illustration of the reduction of the depletion width due to an increased doping density. The Fermi energy in figure (b) is lifted compared to figure (a). Image adapted from [8].

that initial deposition of a thin Ni-film with a thickness of 0-10nm prior to the evaporation of Au/Ge/Ni demonstrates dramatically improved ohmic contacts, which can be reproduced [10].
Instead of Ni, Pd or Pt can also be used as a component, since all elements share the same group in the periodic table of the elements. Indeed, ohmic contact recipes to *GaAs* containing Ni, Pd or Pt were compared [11]. For this purpose 43 nm Ge/ 30 nm Ni(Pd,Pt)/ 87 nm Au was evaporated successively on the *GaAs* device. The samples where Pt was used showed the best electric characteristics. In addition TEM images showed a smooth surface for Au/Pt/Ge while grains where formed for Au/Ni/Ge and Au/Pd/Ge.

1.2.3 Annealing mechanism

In general, the detailed process during the annealing mechanism is not understood. Studies showed that Ge-rich spikes protrude into the *GaAs* and the contact is formed through these spikes. However it is still debated, whether ideal contact is formed via these spikes or via smooth contact surfaces alloyed in the *GaAs* heterostructure [12].
The detailed annealing mechanism was studied recently for contacting AuGe/Ni/Au to the 2DEG of a *GaAs/AlGaAs* heterostructure [13]. Therefore Transmission Electron Microscopy (TEM) and Energy Dispersive X-ray (EDX) was used to visualize the contact formation at several stages of the annealing process. Evidently, a complex structure containing Au- and Ni-rich grains is formed. These grains penetrate through the *GaAs* surface but do not necessarily need to contact the 2DEG to form an ideal contact. For over annealing it was reported that the Au-rich phase diffuse below the Ni-phases leading to an increased ohmic contact resistance. From these findings it was possible to develop a model, which predicts the optimal parameters for contacting a 2DEG.
At low temperatures, TEM studies for Ni/Ge/Au/Ni/Au contacts to a 2DEG embedded in a *GaAs/AlGaAs* device showed that the contact was established predominantly through the formation of spikes [14]. The images distinguished between spikes contacting the 2DEG, spikes being too short and spikes, which penetrated too far into the device. Generally, the first kind of spikes belonged to contacts with the lowest resistances, which decreased monotonically when cooling down. Spikes, which were too short to contact the 2DEG, also showed a monotonically decreasing resistance when cooling, but only until 120K. Therefore the resistance for these kind of contacts was higher at low temperatures, which could be compensated by illuminating the sample. For contacts with spikes that penetrated too deep, a very high resistance was already observed at room temperature and the contacts eventually became insulating when cooling down.

2 Fabrication of the ohmic contacts

2.1 Wafers used

Two different $GaAs/AlGaAs$ heterostructures, referred to as Pinto 15 and 16, were used for studying the ohmic-contact fabrication recipes. Both wafers were grown by Antonio Badolato in the Wegscheider group at the University of Regensburg. Figure 4 shows the growth profile for the two wafers, which were grown by molecular beam epitaxy (MBE). In both structures two 2DEGs are formed: an inverted 2DEG at the interface between the $AlGaAs$ spacer layer and $GaAs$ tunnel barrier as well as a 2DEG at the $AlGaAs/GaAs$-buffer layer interface. The red layers indicate the location of self assembled $InAs$ quantum dots. In this project high density (HD) wafers containing the quantum dots and low density (LD) wafers without the quantum dots were used. The distance from dots to the inverted 2DEG is referred to as the tunnel barrier and defines the tunneling rate from the 2DEG into the self-assembled quantum dots. Both structures reveal a different thickness of the spacing layer, which is the distance of the $Si-\delta$-doping to the 2DEG. The thickness of the layer strongly influences the density of the 2DEG. By decreasing the spacer layer thickness the tunneling rate increases which results in a higher density of the 2DEG. However, the ionized Si donors are a relevant source of scattering and therefore the mobility of the 2DEG is strongly affected when decreasing the thickness of the spacer layer. A relatively thick $AlGaAs$ blocking barrier prevents charge transfer between the quantum well and the surface of the layer, which is important when using top gates. Furthermore, the thickness of the blocking barrier has as well an influence on the density of the 2DEG. The top $GaAs$ layer has the function of a capping layer and protects the underlying $AlGaAs$ layer from oxidation. Compared to Pinto 15, Pinto 16 contains an additional $AlGaAs$ sacrificial layer which can be etched when requested.
Figure 5 shows the conduction band of Pinto 16 obtained when solving the Poisson and the Schrödinger equation for specified layer thicknesses and material properties ($GaAs$ or $AlGaAs$ and Al content) [15]. According to the growth profile a 2DEG forms 152 nm and 282 nm below the surface due to the formation of a quantum well at the $GaAs/AlGaAs$-interface. The δ-doping layer causes a charge dipole between the surface and the doping layer as well as between the doping layer and the heterointerface. Both dipoles result in an electric field which gives constant slopes of the conduction band (fig. 5).

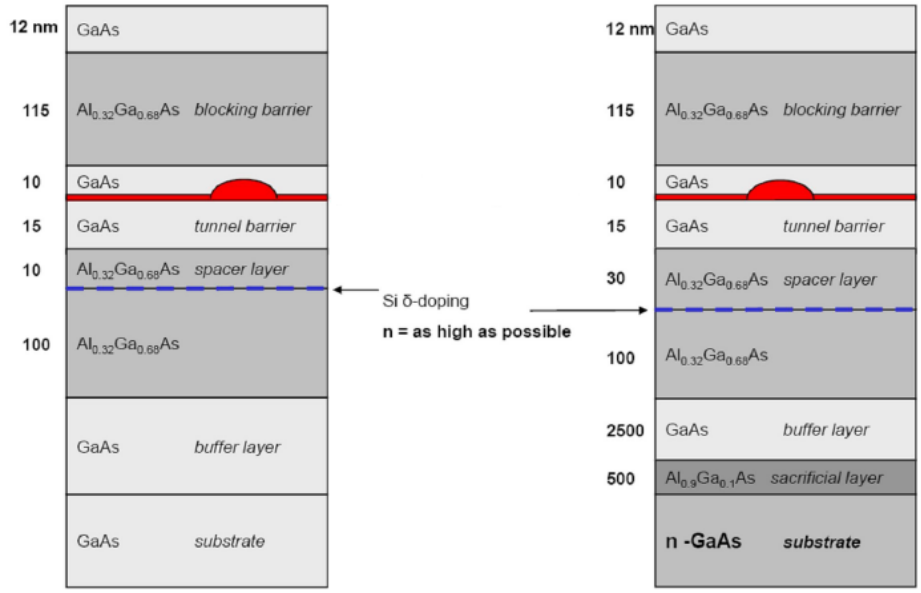


Figure 4: Growth profile of Pinto 15 (left) and 16 (right), grown by molecular beam epitaxy (MBE). The main difference is the location of the δ-doping layer with respect to the 2DEG. In addition a sacrificial $AlGAs$ layer is implemented in Pinto 16.

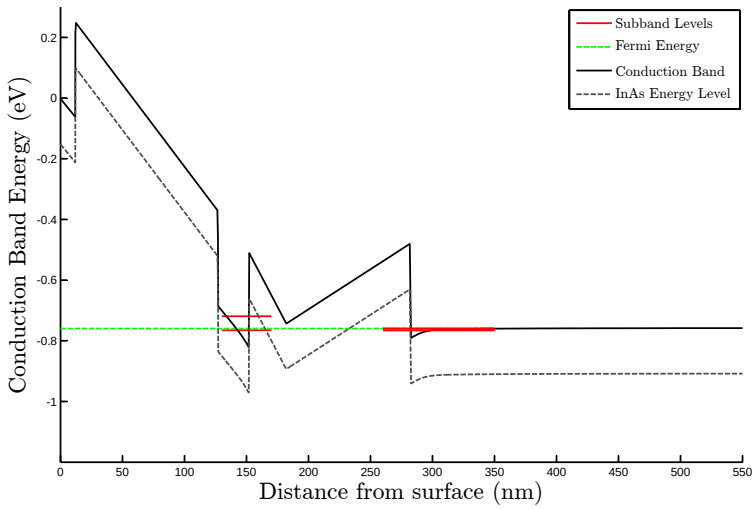


Figure 5: Conduction band structure of Pinto 16. A quantum well forms when the conduction band is below in energy than the fermi energy Graph provided by F. Dettwiler.

2.2 Fabrication

For all wafers the following main steps were pursued in the fabrication (For a detailed fabrication protocol see appendix):

1. Optical lithography of the mesa pattern
2. Etching of the mesa pattern
3. Optical lithography of the ohmic contacts
4. Evaporation of the ohmic contacts
5. Annealing
6. Wire-bonding

To define the mesa structures by optical lithography, negative photoresist (ma-N 415) was spin-coated on the pre-cleaned samples. The photoresist is hardened and therefore insoluble when exposed to light, while the unexposed regions dissolve during the development. A mask precisely defines which areas are unexposed during the lithography. After illuminating and developing, the remaining resist represents the mesa pattern and protects the underlying area from being etched (fig. 6a). Thus the etched mesa pattern was initially defined by the layout of the mask.
For the etching a mixture of $H_2SO_4 : H_2O_2 : H_2O$ with a ratio of 2:16:480 was used. Thereby the hydrogen peroxide acts as the oxidizing agent while the sulfuric acid dissolves the resulting oxide. The etching rate was determined to be ∼140 nm/min, which is in good agreement with literature values [16]. Pinto 15(16) was etched 280(300) nm until the $GaAs$ buffer layer. This is necessary, since etching until the $AlGaAs$ layer only, may cause lift-off problems due to the oxidation of $AlGaAs$. After the mesa etch and removing of the photo resist with NMP, the samples were spin coated with negative photo resist again to define the ohmic contacts.

In figure 6b the wafer is shown after the photo lithography of the ohmic contacts. The bright spots indicate the location of ohmic contacts, while the rest is covered with photoresist. The samples were then treated with oxygen plasma in order to clean impurities on the resist. Before evaporation two different procedures were distinguished. For the one procedure, the samples were dipped into HCl prior to the evaporation to remove remaining oxides from the oxygen plasma. For the other procedure the samples were dipped into a mixture of $H_2SO_4 : H_2O_2 : H_2O$ with the ratio of 1:8:1000 corresponding to a etching rate of ∼40 nm/min. The goal of this pre-etching was to increase the roughness at the ohmic contact spots, which may has an effect on the adhesion of the metals as well as on the diffusion during the annealing cycle.
During the evaporation process Au/Ge/Au/Ge/Pt with thicknesses 120 nm/60 nm/120 nm/60 nm/85 nm were deposited successively on the surface starting with Au. Hereby the Au/Ge builds the eutectic mixture and Pt prevents the 'balling up' from Au/Ge. After the evaporation, the lift-off was done by putting the samples into warm NMP. NMP dissolves hardened negative photo resist and therefore the deposited metal is removed except for the ohmic contact spots, which were not covered by the photoresist (fig. 6c). In the annealing cycle the samples were first heated to 370°C for 2 min to melt the eutectic mixture. Subsequently, the samples were annealed at 420°C, 450°C, 480°C or 510°C for 1 min (fig. 6e). Note that the ohmics only form contact with the 2DEG only on spots with underlying mesa pattern. In the other regions it was etched into the $GaAs$ buffer layer and hence no 2DEG is present there. These contacts are used to implement the top gates, which were not required for this project. The last step was to wire bond the ohmic contacts using Al wire.

A different lift-off behavior was observed for Pinto 16 LD which was dipped into HCl and Pinto 16 LD which was pre-etched prior to the evaporation. Generally sticking problems occurred more often to the sample treated with $H_2SO_4 : H_2O_2 : H_2O$ (fig. 7). Such problems can occur, when the photoresist was underdeveloped. This is not the case here since both structures were processed following the exact same protocol. Moreover, the adhesion problems could be due to the possible oxidation of the $AlGaAs$ for Pinto 16 LD treated with $H_2SO_4 : H_2O_2 : H_2O$. This would imply that at least the whole capping layer of 12 nm thickness was etched away. At first sight this seems rather unlikely since the etching time was chosen in accordance with the determined etching rate so that only 5 nm are etched. However it is possible that the etching rate is not uniform in time and that in fact more than 5 nm were etched. In figure 7b the ohmic spots at the mesa are indeed brightened, which could indicate a too high etching.

2.3 Measurement

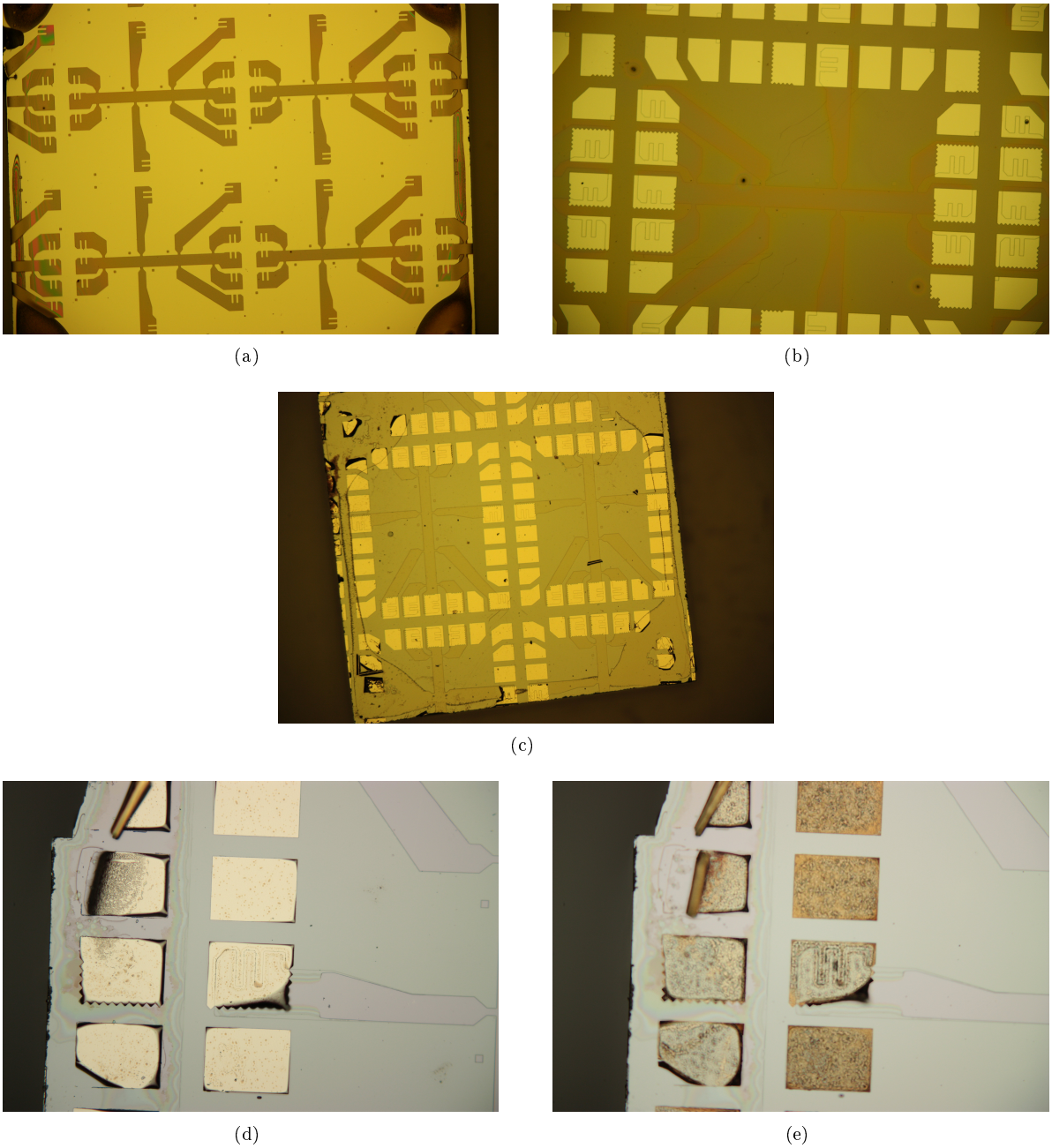
The ohmic contact resistances were measured at room temperature and at 4K using a helium dewar dipstick setup. In addition the samples were also illuminated to increase the density of the 2DEG. Two different measurement techniques were used: the battery measurement and the lock-in technique. When using the battery measurement a known voltage of 10 mV was applied to the sample via the contact to be measured. By measuring the current through the sample the resistance could be determined using Ohm's law. The measured resistance consists not only of the resistance of the ohmic contact but also of the resistance of the battery as well as of the resistance of the dipstick wiring. Since the remaining ohmics were put on ground current also flowed through these contacts and the total measured resistance is given by:

$$R_{meas} = R_{wire} + R_{batt} + R_{ohm} + R_{rest} \tag{7}$$

The resistance of the wires R_{wire} and the battery R_{batt} were determined to be 220 Ω and 9.107 kΩ respectively. The remaining ohmic contacts were all connected to the ground, which means that they are connected in parallel. Therefore, the resistance R_{rest} can be describes as:

$$\frac{1}{R_{rest}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + ... \tag{8}$$

where R_1, R_2, R_3 and so forth represent ohmic contacts which are not measured. It is obvious that R_{rest} decreases the more contacts are connected in parallel. Therefore, the R_{rest} is neglected and we determine the resistance of one specific ohmic using:

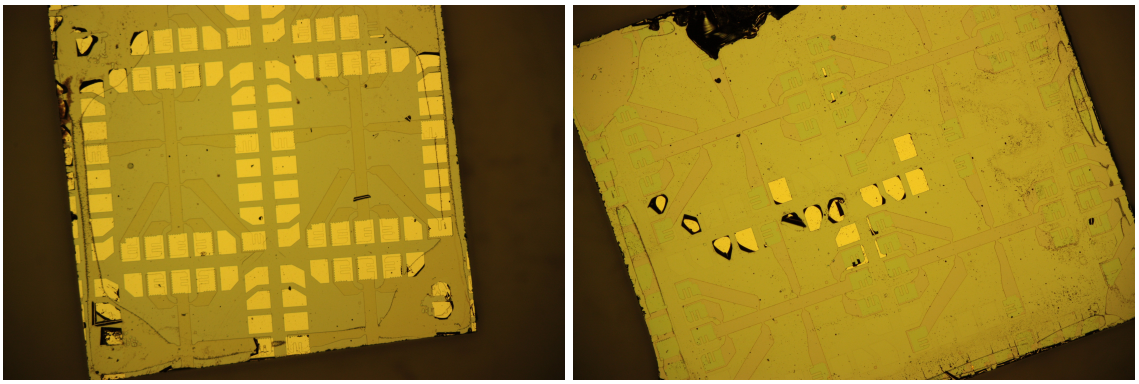


(a) (b)

(c)

(d) (e)

Figure 6: Optical images of different steps during the fabrication process. (a) After photo lithography of the mesa pattern. (b) After etching of the mesa pattern and the photo lithography of the ohmic contacts. The bright spots indicate the location of the ohmic contacts. The shape of the etched mesa pattern is still recognizable underneath the photoresist. (c) After evaporation of Au/Ge/Au/Ge/Pt and lift off in warm NMP. (d) Sample before the annealing process and (e) after the annealing process using an annealing temperature of 510°C. The metal structures on the mesa show a jagged structure, which should improve the annealing of the ohmic contacts.



(a) (b)

Figure 7: Comparison of the lift off for Pinto 16 LD dipped in HCl (a) and Pinto 16 LD pre-etched (b). Obviously, lift-off problems occurred for the pre-etched sample, which could be due to the oxidation of $AlGaAs$. The brightened spots in (b) indeed indicate that more than 5 nm was etched.

$$R_{ohm} = R_{meas} - R_{wire} - R_{batt} \tag{9}$$

When using the lock-in technique, an AC - current of 10.17nA was applied to the sample and the resulting voltage was measured. The lock-in acts as an extremely narrow band-pass filter allowing to filter noise components at unwanted frequencies resulting in a more accurate measurement. To calculate the specific ohmic contact resistance only the resistance of the wire R_{wire} was subtracted from the measured resistance R_{meas} since no battery was present. However, the measurements did not reveal any significant differences between the battery and the lock-in measurements.

3 Results

3.1 Dependence on the annealing temperature

In figure 8a the average ohmic contact resistance of Pinto 15 HD is plotted as a function of annealing temperature measured at room temperature (RT) and at 4K. The resistance seems to be optimal for an annealing temperature of 450°C and increases when further increasing the annealing temperature. A similar behavior was also reported for Au/Pt/Ge ohmics, which also showed optimal resistances for samples annealed at 450°C [11]. Furthermore, the resistances measured at room temperature were much lower than for measurements performed at 4K. Such an effect is clearly not expected since low temperatures should minimize scattering effects and hence decrease the resistance. However, it is possible that the ohmic did not make contact to the 2DEG during the annealing mechanism resulting in a increased resistance for low temperatures as reported earlier [14].
Figure 8b shows the average ohmic contacts resistance for Pinto 16 LD at 4K. Compared to Pinto 15 HD the resistances are much lower and seem to further decrease by increasing annealing temperature. The lower data points reveal the measured resistances at 4K after illuminating the sample for 1 min. The resistance is obviously dramatically decreased due to the additional charge carriers, which were excited into the 2DEG. Generally the resistances of Pinto 15 HD were much higher than the resistances measured for Pinto 16 LD at 4K, while at room temperature the resistances were comparable. For example at an annealing temperature of 450°C the resistances of Pinto 15 HD are around 30 kΩ while for the non-illuminated Pinto 16 LD samples the resistance was determined to be around 500 Ω. This difference maybe a consequence of the relatively small spacer layer, which strongly affects the mobility of the 2DEG in Pinto 15HD (fig. 4). However, as mentioned above, a poor contact to the 2DEG could also be the reason of this observation.

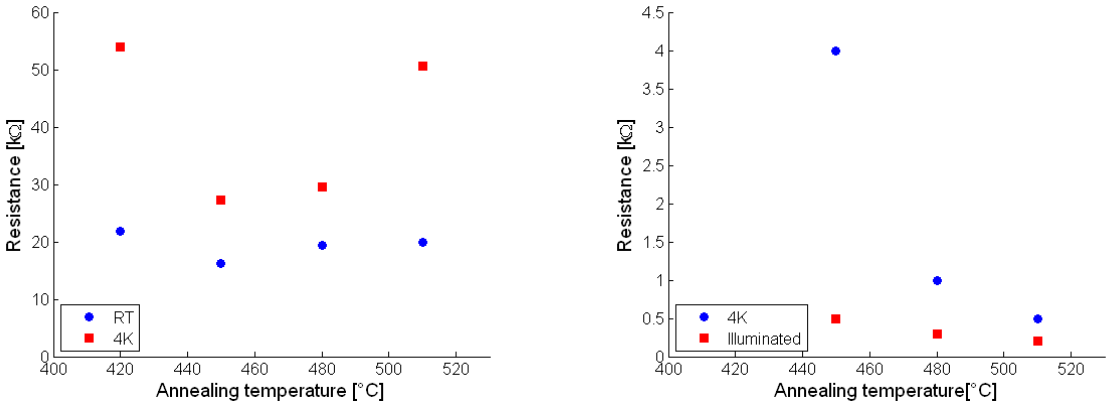


Figure 8: Dependence of the ohmic contact resistances on the annealing temperature. (a) Pinto 15 HD measured at room temperature (RT) and at 4K. (b) Pinto 16 LD measured at 4K before and after illumination by a LED.

3.2 Effect of etching prior to evaporation

The effect of etching the ohmic contact spots prior to the evaporation was studied using Pinto 16 LD annealed at 480°C and 510°. Thereby Pinto 16 LD rinsed in HCl before the evaporation was compared to Pinto 16 LD etched prior to the evaporation using a mixture of $H_2SO_4 : H_2O_2 : H_2O$. Table 1 summarizes the results obtained from this comparison.
Evidently, the ohmic resistance of the pre-etched samples is not lower compared to the ohmics rinsed in HCl. This implies that the pre-etching had no influence during the annealing mechanism. In contrary, the resistances are even as twice as high for measurements on non-illuminated as well as illuminated samples. The reason for this observation is not quite clear. A possible explanation could be that the $AlGaAs$ layer

Sample	Annealing temperature [°C]	Resistance 4K before illuminating [kΩ]	Resistance 4K after illuminating [kΩ]
Pinto 16 LD	480	∼1.0	∼0.3
(rinsed in HCl)	510	∼0.5	∼0.2
Pinto 16 LD	480	∼2.0	∼0.6
(pre-etched)	510	∼1.9	∼0.4

Table 1: Comparison between the samples etched before the evaporation and the samples treated with HCl.

was oxidized during the process. However, the $GaAs$ capping layer should not be etched away completely during the pre-etching. Further it is rather unlikely that the etching of the surface influenced the actual electron mobility of the 2DEG since only a few nanometers were etched.

To test the roughness of the etched areas, the pre-etched samples were investigated using atomic force microscopy (AFM). Figure 9 shows the height image of a sample, where the ohmic pad came off during liftoff and the evaporated metals were removed. The image was recorded on the mesa along a jagged edge, whereby the triangle at the upper part was covered by photoresist and hence was not affected when treated with $H_2SO_4 : H_2O_2 : H_2O$. To estimate the roughness of the surface the root mean square (rms) values were measured. For the triangle an rms value around 2.0 nm was obtained, while the rms of the pre-etched area was determined to be around 2.5 nm. This implies that the pre-etching effectively increases the roughness of the sample. In addition, it is clearly visible that the edge does not appear sharp in the AFM image, which is most likely due to the anisotropic etching behavior of $H_2SO_4 : H_2O_2 : H_2O$.

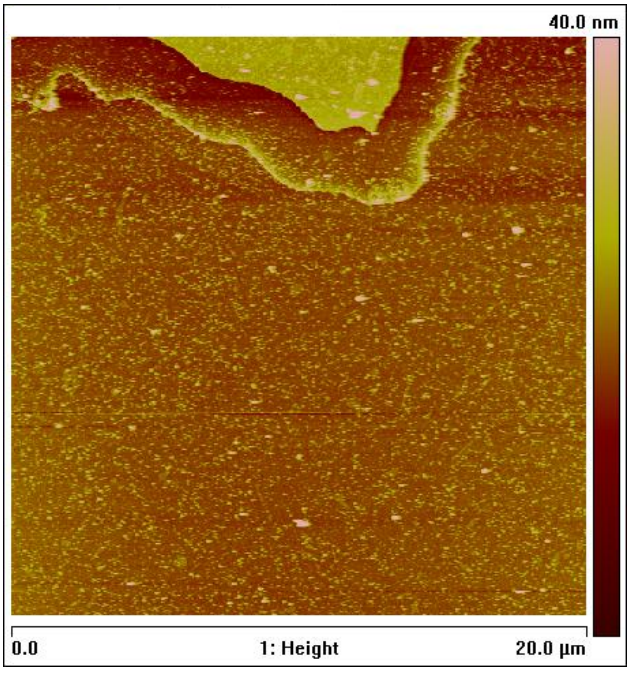


Figure 9: Height image of the surface of a pre-etched sample. The image was recorded on the mesa pattern, while the upper triangle defines a region which was covered with photoresist during the pre-etching of the sample

The measured height difference between the two different regions was determined to be around 7 nm. This value is in good agreement with the calculated etching depth estimated according to the determined etching rate. Furthermore, that finding implies that the $GaAs$ capping layer was not removed during the etching process and hence it seems unlikely that oxidation of the $AlGaAs$ reasons the decreased ohmic contact

resistance of the pre-etched samples.
Figure 10 shows a zoom in on the etched and non etched area. The rms values for these images were determined to be around 0.21 nm for the non-etched (left side of figure 10) and 0.36 nm for the etched area (right side of figure 10). Note that these rms values differ from the values obtained from figure 9 by a factor of ten due to the higher resolution obtained in figure 10.

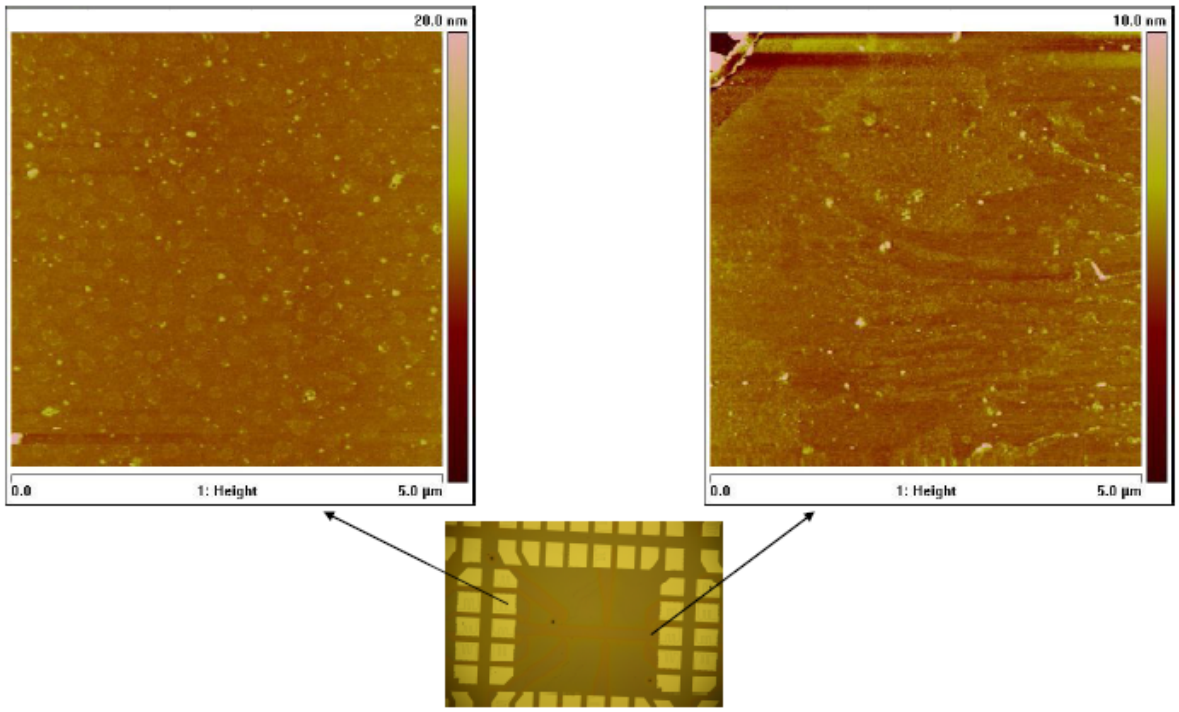


Figure 10: AFM measurements of the areas, which were pre-etched surface (left) and the non-etched areas (right). The photograph was taken before the sample was treated with $H_2SO_4 : H_2O_2 : H_2O$ and illustrates which positions of the mesa were examined with the AFM.

3.3 Conclusion

The ohmic contact recipe using Au/Ge/Au/Ge/Pt was shown to be successfully implemented. The measurements showed quite some difference between Pinto 15 and Pinto 16 at 4K: While measurements for Pinto 15 revealed resistances between 54 and 27 kΩ, resistances lower than 1.0 kΩ were obtained for Pinto 16. In contrary, room temperature measurements showed resistances around 20 kΩ for both wafers. Furthermore the annealing temperature for Pinto 15 wafers seem to have an optimum around 450°C, while for Pinto 16 the resistances seem to decrease further with increasing the annealing temperature. The difference in resistance between Pinto 15 and 16 is not clearly understood. A possible explanation could be that the δ-doping layer is located closer to the 2DEG in Pinto 15. This would decrease the mobility of the electrons in the 2DEG, since the Si-donors are a relevant source of scattering. However, locating the δ-doping layer closer to the 2DEG could also increase its density, which would be observable in a lowered resistance. However to understand the exact behavior of these two counteracting effects, a systematical study using several different wafers with a different spacer layer thickness would be necessary.
Another possible explanation of the difference in resistances could be that the ohmics on the Pinto 15 wafers do not form proper contacts to the 2DEG during the annealing process. This could be the reason, why the resistance is increased when cooling down: charge carriers which contributed to the current at room temperature are now frozen in, while the reduction of scattering effects in the 2DEG has little effect due to the lack of proper ohmic contact. However, this reasoning assumes that the annealing mechanism for Pinto 15 differs from the annealing mechanism in Pinto 16. This is rather unlikely, because the growth profile from the surface to the 2DEG is identical for both wafers (assuming we measure the inverted 2DEG). Similarly a consequence of overannealing for the Pinto 15 wafers can be excluded for the same reason.
It is further unclear, whether the presence of self assembled quantum dots has an influence on the resistance measurements presented above. Unfortunately it was not possible to directly compare wafers with dots to identical wafers without dots. Such a comparison is insofar interesting for potential future experiments using electrons trapped in the self-assmbled $InAs$ quantum dots.

Pre-etching the samples prior to the evaporation did not have the anticipated effect. In contrary it was reported that the resistance even increase when treating the sample with $H_2SO_4 : H_2O_2 : H_2O$. The reason for this is unclear since oxidation of the $AlGaAs$ layer should not occur and the etching should also not affect the electron mobility in the 2DEG. Furthermore, more lift-off problems were experienced when the samples where pre-etched. However, the AFM images confirm rougher surfaces for pre-etched samples but it seems that this does not influence the annealing mechanism.

The achieved resistances below 1.0 kΩ in Pinto 16 wafers is already quite low. However, it is desirable to have minimized ohmic contact resistances. Generally, the composition of the recipe can be alternated to improve the ohmic contacts. A possibility would be to study the effect of different annealing times on the ohmic contact resistances. Moreover, since the resistance of Pinto 16 wafers seem to further decrease with increasing annealing temperature, an opportunity would also be to use higher annealing temperatures. Alternatively, the composition of the metals used could also be varied by introducing a wetting layer for example, which could increase the adhesion of the metals. However, since the annealing mechanism is mainly remains unclear it is rather difficult to state concrete proposals in order to improve the ohmic contacts.

Acknowledgement

Primarily, I would like to thank Florian Dettwiler, who explained me all the machines used for fabrication and for being always helpful and patient when I had problems. I would also like to acknowledge Prof. Dominik Zumbühl for giving valuable inputs on the project and for the possibility to accomplish this project within his group. Further thanks go to Antonio Badolato from the Wegscheider group for providing us with the heterostructures. Finally, I would like to thank all the group members of the Zumbühl group for always being willing to answer my questions.

References

[1] von Klitzing K., Dorda G., Pepper M. New Method for High-Accuracy Determination of the Fine Structure Constant Based on Quantized Hall Resistance. *Physical Review Letters* **45** (6), 1980

[2] Tsui D.C., Stormer H.L., Gossard A. C. Two-Dimensional Magnetotransport in the Extreme Quantum Limit. *Physical Review Letters* **48** (22), 1982

[3] van Wees B.J., van Houten H., Beenakker C.W.J., Williamson J.G., Kouwenhoven L.P., van der Marel D., Foxon C.T. Quantized Conductance of Point Contacts in a Two-Dimensional Electron Gas. *Physical Review Letters* **60** (9), 1988

[4] Loss D., DiVincenzo D. P. Quantum Computing with quantum dots. *Physical Review A* **57** (1), 1998

[5] For a review see for example: Hanson R., Kouwenhoven L.P., Petta J.R., Tarucha S., Vandersypen L. M. K., Spins in few-electron quantum dots. *Reviews of Modern Physics* **79**, 2007

[6] Zumbühl D. Introduction to Mesoscopic Physics and Quantum dots *Lecture at the Institute of Physics, University of Basel* HS 2008

[7] Oberholzer S. Nano-Elektronik. *Lecture at the Institute of Physics, University of Basel* HS 2007

[8] Look D.C. Electrical Characterization of GaAs Materials and Devices. *Design and Measurement in Electronic Engineering* (1988)

[9] Göktas O., Weber J., Weis J., von Klitzing K. Alloyed ohmic contacts to two-dimensional electron system in AlGaAs/GaAs heterostructures down to submicron length scale. *Physica E* (2008) 1579-1581

[10] Valeille A., Muraki K., Hirayama Y. Highly reproducible fabrication of back-gated GaAs/AlGaAs heterostructures using AuGeNi ohmic contacts with initial Ni layer. *Applied Physics Letters, 92, 152106 (2008)*

[11] Lin C., Lee C.P., Comparison of Au/Ni/Ge, Au/Pd/Ge and Au/Pt/Ge Ohmic contacts to n-type GaAs. *J.Appl. Phys.* **67**(1), 1990

[12] Fleischer M. Transporteigenschaften von Quantenpunktkontakten und Quantenpunkten. *Dissertation* Eberhard Karls Universität zu Tübingen (2006)

[13] Koop E.J., Iqbal M.J., Limbach F., Boute M., van Wees B.J., Reuter D., Wieck A.D., Kooi B.J., van der Waal C.H. The annealing mechanism of *AuGe/Ni/Au* ohmic contacts to a two-dimensional electron gas in $GaAs/Al_xGa_{1-x}As$ heterostructures. *arXiv:0809.0928* (2008)

[14] Taylor R.P., Coleridge P.T., Davies M., Feng Y., McCaffrey J.P., Marshall P.A. Physical and electrical investigation of ohmic contacts to AlGaAs/GaAs heterostructures. *J. Appl. Phys.* **76** (12), 1994

[15] Dettwiler F. Fabrication of Lateral Self-Assembled Hybrid Nanostructures. *Master's Thesis* 2008

[16] Williams R. Modern GaAs Processing Methods. *Artech House* 1994

A Appendix - Fabrication protocol

Optical lithography of the mesa pattern

- cleaving $GaAs/AlGaAs$ with diamond scribe
- clean samples: 3 solvent clean: 5 min. TCE, 5 min. Acetone, 5 min. Methanol each in ultrasound
- blow off samples with N_2
- pre-bake samples on hot plate: 120°C for 5 min., let cool for 2 min.
- spin photoresist (ma-N415), 6000 rpm, 40s, ramp time: 6s
- bake on hot plate 93°C, 90s
- expose on mask aligner: for 7.0s, use hard contact time 2.0s, pressure: 1.4 bar
- develop for 60s in developer (ma-D 332S)

Etching of the mesa pattern

- measure thickness of the resist with α - stepper
- prepare etching solvent $H_2SO_4 : H_2O_2 : H_2O$ mixture 2:16:480
- determine etching rate by etching a test sample for 1 min. and measure depth with α - stepper
- etch 280 nm (Pinto 15) 300 nm (Pinto 16)
- remove resist: put samples into warm NMP (45°-50°C)
- verify etching depth using α - stepper
- blow off with N_2 gun

Optical lithography of the ohmic contacts

- 3-solvent clean and prebake at 120°C for 5 min
- spin photoresist (ma-N415), 6000 rpm, 40s ramp time; 6s
- bake at 93°C for 90s
- align sample with ohmic pattern on the mask
- expose on mask aligner: for 7.0s, use hard contact time 2.0s, pressure: 1.4 bar
- develop 60s in developer (ma-D 332S)
- check with optical microscope develop longer if necessary

Evaporation of the ohmic contacts

- prepare etching solvent $H_2SO_4 : H_2O_2 : H_2O$ 1:8:1000 and calibrate etching rate
- calibrate oxygen plasma using a test sample covered with photoresist illustrating a mesa pattern
- etch $\simeq$40 nm with oxygen plasma
- Choose between following steps:
  - dip sample 5s in HCl rinse in DI H_2O
  - etch 5 nm in $H_2SO_4 : H_2O_2 : H_2O$ 1:8:1000 and rinse in DI H_2O
- load sample into evaporator, pumping, cooling down to 0°C
- evaporate successively:
  - 120 nm Au
  - 60 nm Ge
  - 120 nm Au
  - 60 nm Ge
  - 85 nm Pt
- lift off in warm NMP for 30 min. clean with syringes

Annealing & wire bonding

- anneal samples:
  - 2min. 370°C
  - 1 min. 420°C, 450°C, 480°C or 510°C
- cleave samples if requested
- wire bonding using Al wire