Master thesis

A study on low-resistance contact formation with diamond using metal containing high amount of impurities

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ABSTRACT

Diamond has excellent properties as wide band gap, high thermal conductivity, high breakdown voltage, and both high electron and hole mobilities. Taking these good properties into account, diamond has drawing significant attention as an "ultimate" semiconductor for future electronics with high voltage operation as well as ultrahigh speed operation. One of the issues for diamond electron devices is high contact resistance at the metal and diamond interface. Small contact resistance is an important factor to fabricate high-performance and low-loss devices. *p*-type ohmic contact with boron-doped diamond and titanium can be formed with the contact resistance of 10^{-6} Ωcm^2. On the other hand, *n*-type ohmic contact with small contact resistance has not been realized yet despite various efforts have been done and the current minimum value of contact resistance is 2.2×10^{-3} $\Omega \bullet cm^2$ by using Au/Pt/Ti electrode. The reasons of high contact resistance of *n*-type diamond are large Schottky barrier height (4.6 eV) and Fermi level pinning. In the Si Schottky diode, barrier height can be controlled by putting dopant materials (P or B) at the diamond and metal electrode interface. In this thesis, a novel method to reduce the contact resistance has been proposed by incorporating phosphorus atoms at the interface.

Diamond substrates used in this work include heavily phosphorus-doped *n*-type epitaxial layer at the surface with concentration of 8×10^{19} and over 10^{20} cm^{-3} grown on synthetic Ib diamond substrate. Electrode is a nickel and silicon multi-stacking structure to form $NiSi_2$ by annealing. In this study, Ni and Si films with thicknesses of 0.5 and 1.9 nm, respectively, were cyclically sputter deposited on substrates for 32 repetitions. And the bottom layer was changed to Ni_3P, the Ni_3P layer thickness was 0.7 nm grown by

the sputter deposition. The use of bottom layer was expected that phosphorous is diffused into the diamond surface region and reduce contact resistance.

An increase in reverse diode current has been observed he contact resistance is 7 $\times 10^{-2}\ \Omega\cdot cm^2$ when P incorporated $NiSi_2$ electrodes have been annealed at 850 ^oC. The current is especially significantly increased at a low bias territory (1-2V) in comparison with Ti which is now commonly used as electrode. The reason for this is considered that interface of diamond and Si react to SiC and solid phase doping is occurred close at diamond surface. It has been shown that both Si and P atoms play an important role for effectively tuning the Schottky barrier height.

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Chapter 1
Introduction

1.1 Power electronics and device

Power electronics is a technology that focuses on the power converter and control. As power electronics has been used, there is a semiconductor power conversion device; inverter that converts direct current (DC) to alternating current (AC) and rectifier that converts the DC from the AC. These devices are very widely used electric power sector such as power generation and transmission, industry such as fans and pumps, power supply such as communication systems and plant, electric railway field as the drive train and substation, automotive, and consumer electronics. In recent years considered, it is important to reduce CO_2 and save energy. There is also the problem of economic impact of the rise in fuel costs due to soaring oil.

Power devices that enable high-efficiency power conversion will contribute significantly to the energy conservation. Therefore power device has attracted attention as a key technology to solve the problem of global warming and energy issues.[1], [2]

Power device is semiconductor device to control electrical power. MOSFET or IGBT made of Si is currently widely used as a power semiconductor device. [3] However, these devices using Si are close to the limit performance due to material properties. In particular, Ultra-high efficiency power converter handling high-voltage is necessary to achieve a stable power supply in the future electrical network connected with solar power, wind power and other clean energy sources. Ultra high voltage and low loss power semiconductor devices is the key to do this. However, in existing semiconductor devices of Si have been impossible to achieve, there is a need for discovery of new materials. Wide-gap semiconductor has remarkably excellent properties such as simplified cooling, small size and low loss in power device applications compared to Si.

These devices in the future are expected to be useful as key innovative devices to a low-carbon society creation. Wide gap semiconductor materials are diamond, Silicon carbide (SiC), Gallium nitride(GaN) and so on.[4] In order to achieve ultra-high voltage and low loss device, it is necessary to develop devices that use these wide-gap semiconductor materials.

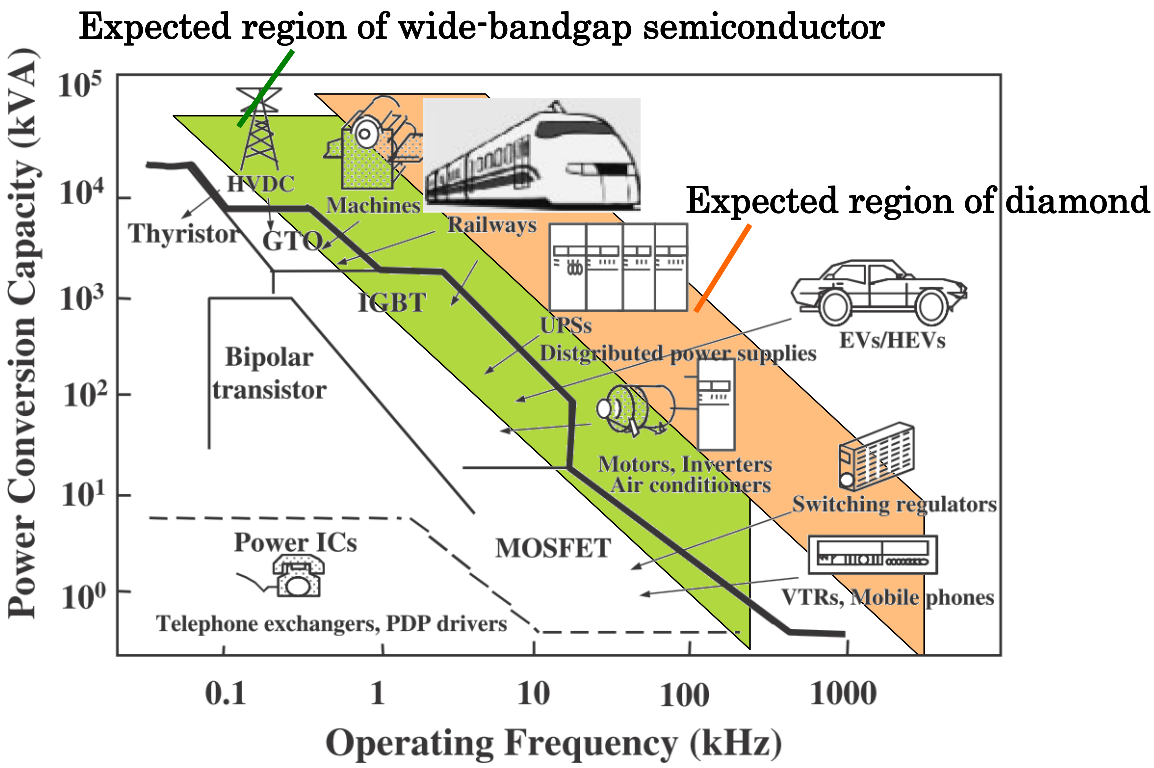


Fig 1-1 Expected region of wide-bandgap semiconductor

1.2 Diamond

Diamond is one of the allotrope of carbon and the hardest natural substance. It is used as gems and abrasives. Crystal structure is octahedral, and there is also a six-sided dodecahedron. Fig 1-1 shows crystal structure of diamond.

Each carbon atoms on the top are bonded by the hybridized sp^3 bond. There is no distortion at all because it is ideal angle geometrically. Bond length is 1.54Å. On the other hand, graphite, one of the allotrope carbon, has layered hexagonal structure and the hybridized sp^2 bond in a layer. Bonding force is relatively strong in one layer because of covalent bond, but Bonding force between layers is weak because of Van der Waals bond.

Since the unpaired electron does not exist in the atoms of the crystal, diamond indicates the nature of the insulator. Electrical conductivity can arise by an impurity doping of such as boron or phosphorous in the manufacturing process.

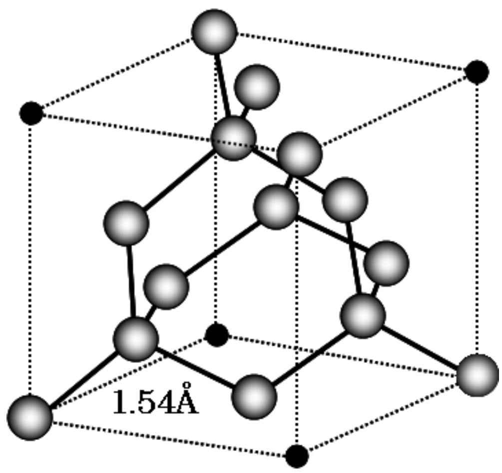


Fig 1-1 Crystal structure of diamond

1.3 Diamond as semiconductor

Band gap of diamond is 5.47 eV and electrical conduction properties of diamond as intrinsic semiconductor is insulator. Diamond semiconductor can be made by doping impurities in the manufacturing process. n-type semiconductor characteristics is obtained by doping phosphorous, p-type semiconductor characteristics is obtained by doping boron. It has been realized to semiconductor device the operating at ultra-high power and frequency, and deep UV LED reflecting its band gap. Currently, it has been reported by Japan NIMS and AIST that pn-junction diamond LED which the emission wavelength of 235 nm by the free exciton[5]. It was reported that p-type semiconductor diamond becomes a superconductor with very low temperature and boron doping concentration over 10^{21} cm^{-3}. [6] The electrical conductivity with concentration over 10^{19} cm^{-3} changes hopping conduction from conduction band. In addition, conduction changes to metallic conductivity almost no activation energy with increasing concentration.

Table 1-1 shows comparison of semiconductor materials properties; diamond, Si, SiC(4H), GaN [7]. Breakdown electric field of diamond is 30 times higher than Si. Therefore diamond can set much higher operating voltage. Since power is the product of voltage and current, diamond can output a higher power in case a high voltage secured. Fig 1-2 shows comparing Si and diamond MOSFET size with ensuring the breakdown voltage of the equivalent. Silicon must be thicker drift region thickness to ensure the high breakdown voltage but at the same time, increases power consumption increasing because of the resistance at the drift region increases. Diamond can be 1/30 of the Si film thickness, because diamond has 30 times higher breakdown field than Si.

Diamond has more than twice electron mobility of Si, the resistance of operating is lower and thus power consumption can reduce. Hole mobility is also high. Diamond has the characteristics that both high mobility of electrons and holes other semiconductor materials do not have. Diamond has excellent heat dissipation because of highest thermal conductivity during all materials. Therefore, diamond device requires less causing the Si device too much during operation and can output higher power.

Tab 1-1 Semiconductor material properties

Material	Si	SiC(4H)	GaN	Diamond
Band Gap (eV)	1.1	3	3.4	5.47
Electron Mobility (cm^2/Vs)	1400	1000	900	2200
Hole Mobility (cm^2/Vs)	600	115	150	1600
Dielectric constant	11.8	9.7	9.0	5.5
Break-down Field (MV/cm)	0.3	2.5	3.3	10
Thermal Conductivity (W/cm·℃)	1.5	4.9	2.0	20.9

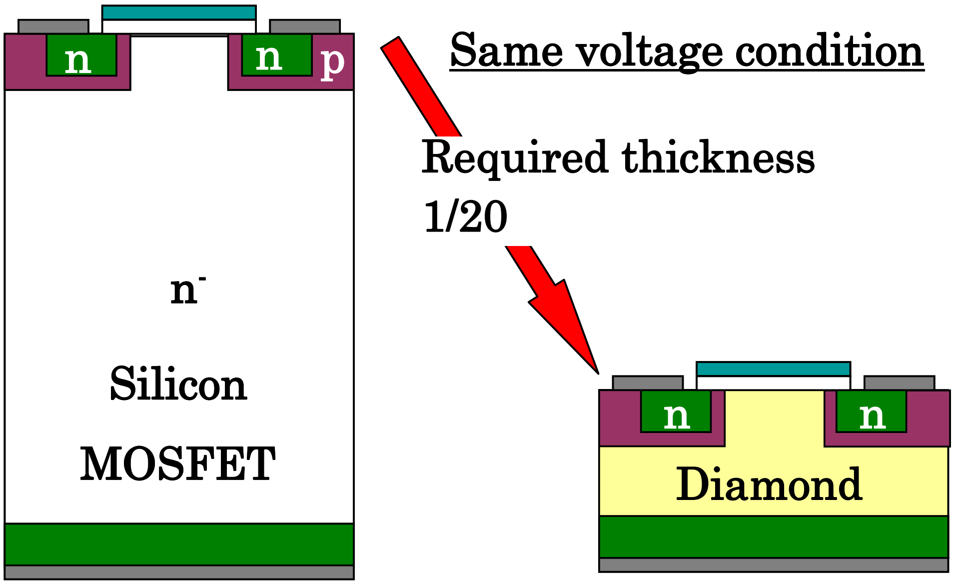


Fig 1-2 Comparing Si and diamond device size with same voltage condition

1.4 Contact Resistance

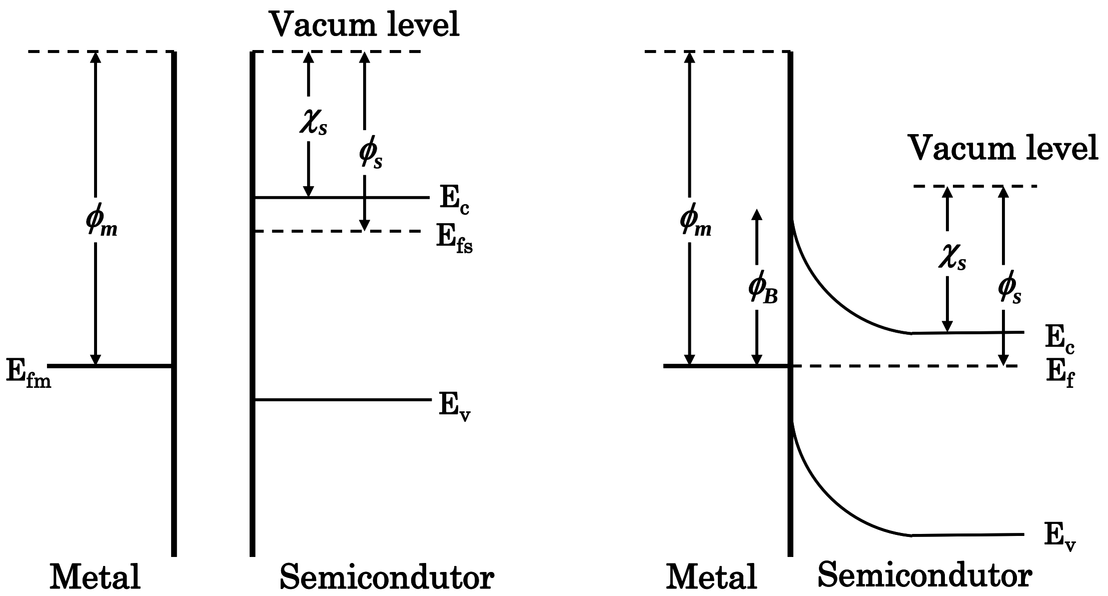
The contact between semiconductor and metal generally induces energy barrier ϕ_B at the interface because of their bandgap difference. Electrical resistance at their interface called contact resistance is generated due to the energy barrier ϕ_B. The metal/semiconductor current-voltage characteristics determined by the height of ϕ_B. It is Schottky or ohmic contact of the magnitude of work function difference.

Figs 1-3 and 1-4 show band diagram of n-type semiconductor and metal contact. ϕ_m is metal work function, ϕ_s is semiconductor work function and χ_s is semiconductor electron affinity. Energy barrier height ϕ_B is written at

$$\phi_B = E_g - (\phi_m - \chi_s) . \qquad (1\text{-}1)$$

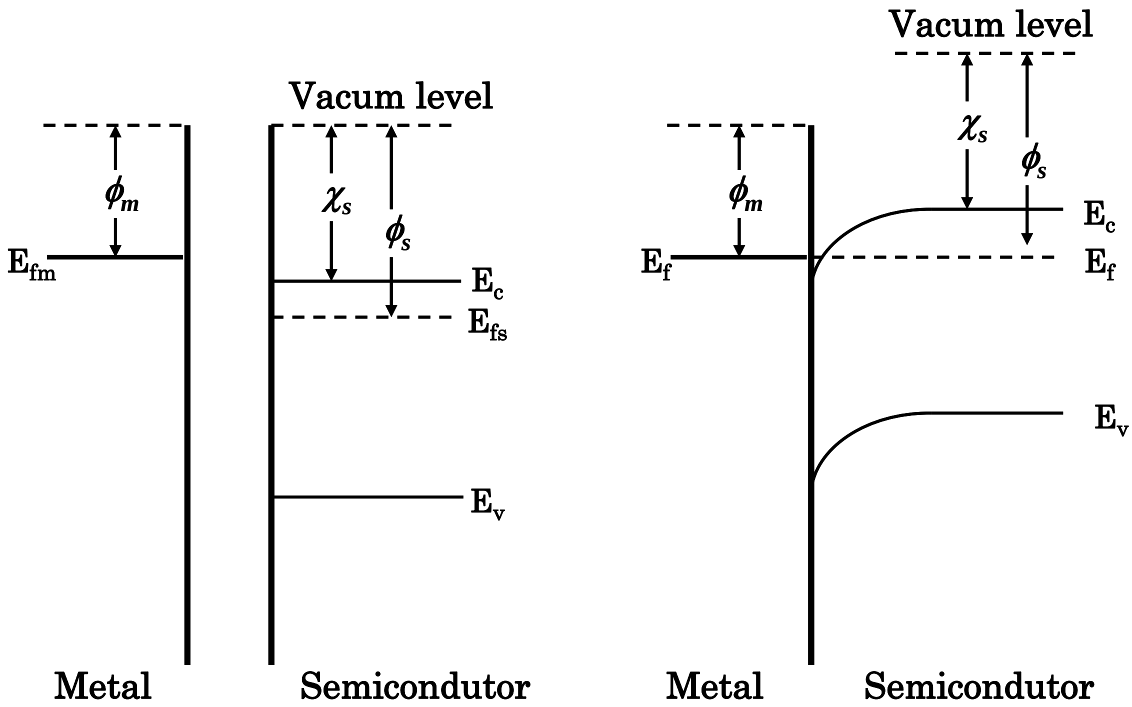
Fig 1-3 is metal / n-type semiconductor contact when $\phi_m < \phi_s$. The situation where contact becomes a Schottky contact. This contact Energy barrier prevents the movement of the carrier. Therefore when the contact of the electrodes and semiconductor to use semiconductor device, as shown in Fig 1-4 is better than Fig 1-3. This contact called ohmic contact. [8]

Since there is no energy barrier in the contact, the current flowing through the semiconductor is determined only by the resistance in Ohm's law this contact is proportional to the voltage and current is established.



(1) Before contact (2) After contact

Fig. 1-3 Band diagram of the metal / n-type semiconductor contact when $\phi_m < \phi_s$



(1) Before contact (2) After contact

Fig. 1-4 Band diagram of the metal / n-type semiconductor contact when $\phi_m > \phi_s$

In addition, as the method for forming the ohmic contact, a method of doping high concentration impurity in the surface layer of the semiconductor is widely used. By the high concentration doping, the depletion width is narrowed. The carrier pass through the barrier by tunneling effect. Therefore the ohmic contact is formed. Performance index of the ohmic contact is represented by the contact resistance ρ_c. contact resistance ρ_c is expressed as

$$\rho_C \propto \exp\left(\frac{\phi_B}{\sqrt{N_A}}\right), \qquad (1\text{-}2)$$

Where N_A is dopant concentration in the semiconductor. In order to obtain low contact resistance, it is necessary either to decrease the energy barrier on increase the dopant concentration.

1.5 Contact Resistance of diamond

A circumstance of the contact is very different in the p-type and n-type diamond. Fig 1-5 shows band diagram of n-type diamond. Schottky barrier height ϕ_B is high in case the contacting metal/n-type diamond because bandgap of diamond is large as 5.47 eV, and doping level E_{fn} is also 0.6 eV away from conduction band E_c. Proportional to ϕ_B, the contact resistance ρ_c of n-type diamond is larger than Si. Metal/n-type diamond contact is happen strong Fermi level pinning, and Schottky barrier height ϕ_B is fixed at about 4.3 eV. Fig 1-6 shows Schottky barrier height versus work function of metal.[9] By this Figure, Schottky barrier height is found to be constant regardless of the work function of the metal at about 4.3 eV. For these reason, Low contact resistance and ohmic contact of n-type diamond have not been achieve. Recently, Titanium is used well as n-type diamond electrode and contact resistance is lowered by increasing the doping concentration of the substrate. When doping concentration is over 10^{19} cm^{-3}, hopping conduction is occurred and this conduction is used to reduce contact resistance. Hopping conduction is transporting by tunnel effect between localized donor levels. The current minimum value of contact resistance is 2.2×10^{-3} $\Omega \cdot cm^2$ by using Au/Pt/Ti electrode. But it has not been reported realizing ohmic contact on n-type diamond. [10]

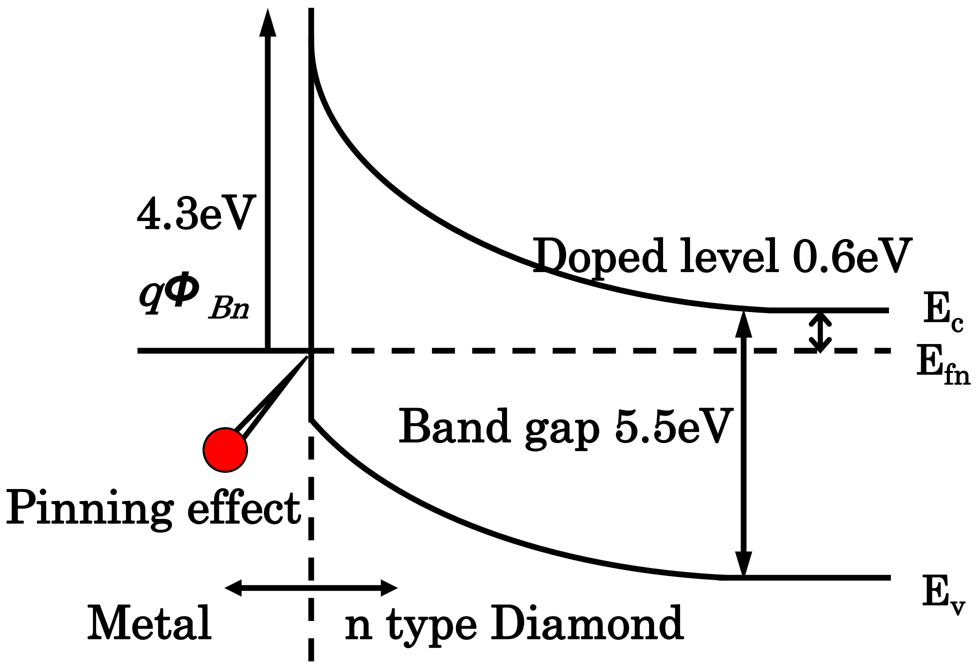
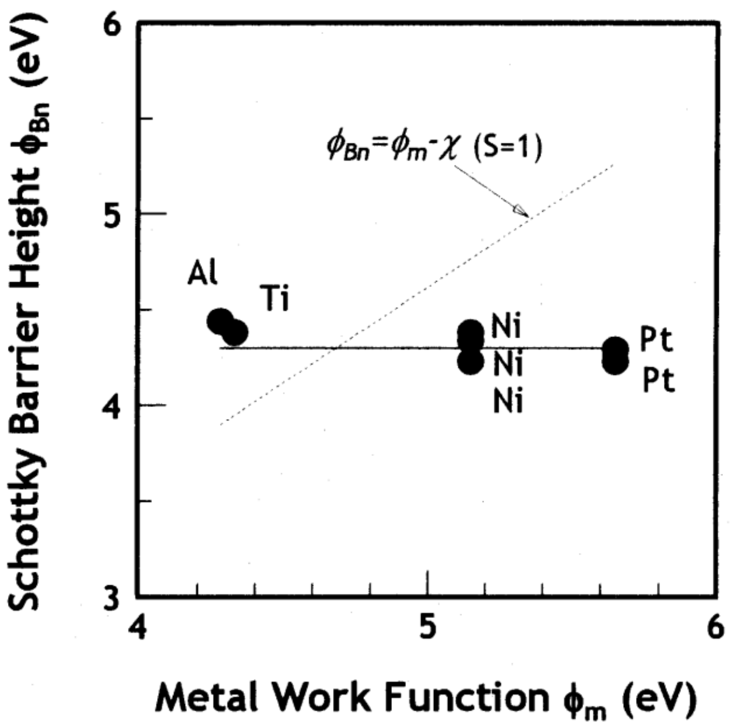


Fig 1-5 Band diagram of n-type diamond



M. Suzuki, S. Koizumi, et al IEICE technical report ED2006-37 [9]

Fig 1-6 Metal work function vs Schottky barrier height of n-type diamond

In regard to p-type diamond ohmic contact and low contact resistance have been realized relatively easily. Fermi level pinning occurs also in the P-type, but the Schottky barrier height is 1.2 eV about 1/4 of the n-type diamond, so we can take the ohmic contact in the pinning state. In p-type diamond contact, it is realized contact resistance $10^{-5} \sim 10^{-6}\ \Omega\cdot cm^2$ and ohmic with using titanium electrode and oxygen-terminated by mixture acid. In this occasion, the ohmic contact is formed by TiC reacting Ti and C at the interface.[11] Interfacial reaction has a great influence in the contact of the diamond. It can be released Fermi level pinning by the hydrogen-terminated such as using hydrogen plasma and also be Schottky contact.

1.6 Multi-stacking Process & Schottky barrier height control

Multi-stacking process obtains compound by alternately depositing two materials and annealing. Fig 1-7 shows image of obtaining $NiSi_2$ from Ni & Si stacking structure. It can get good $NiSi_2$ that these thicknesses are set to achieve 1：2 atomic ratio of Ni and Si. In this process, it is possible to control the composition easily by changing the layer thicknesses during stacking to get down compound forming temperature by facilitating reaction for many layers.

Fig 1-8 shows J-V characteristics of Schottky diode which was contacted $NiSi_2$ and n-type Si substrate.[12] P was Phosphorous incorporated $NiSi_2$ electrodes and B was Boron incorporated $NiSi_2$ electrodes in the figure. The characteristics changed by inserting Phosphorous or Boron. This change indicate modulating Schottky barrier height by semiconductor doping materials as P or B.

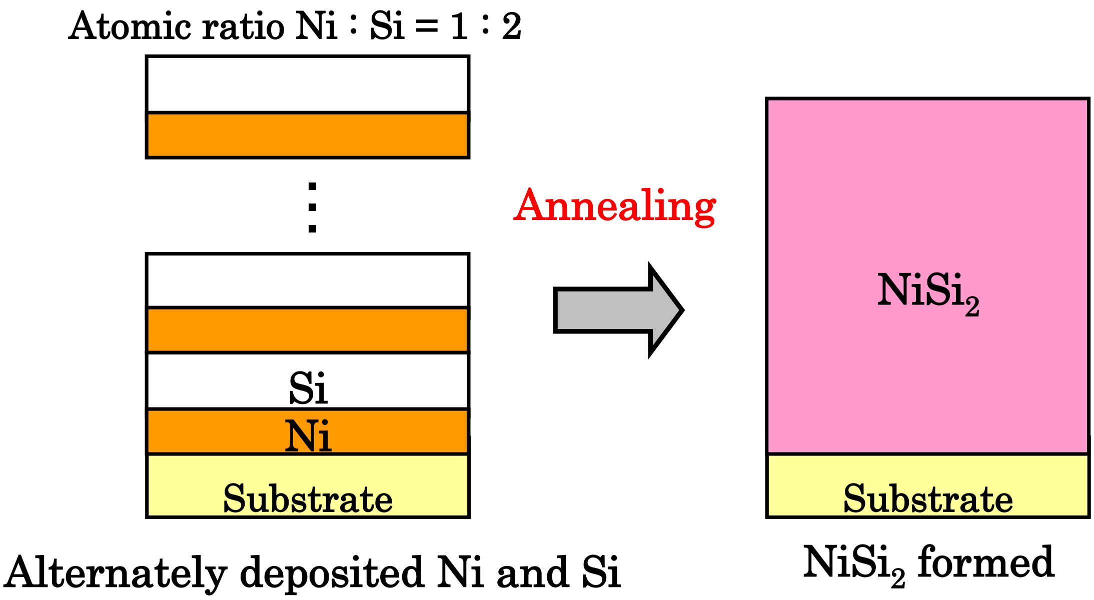
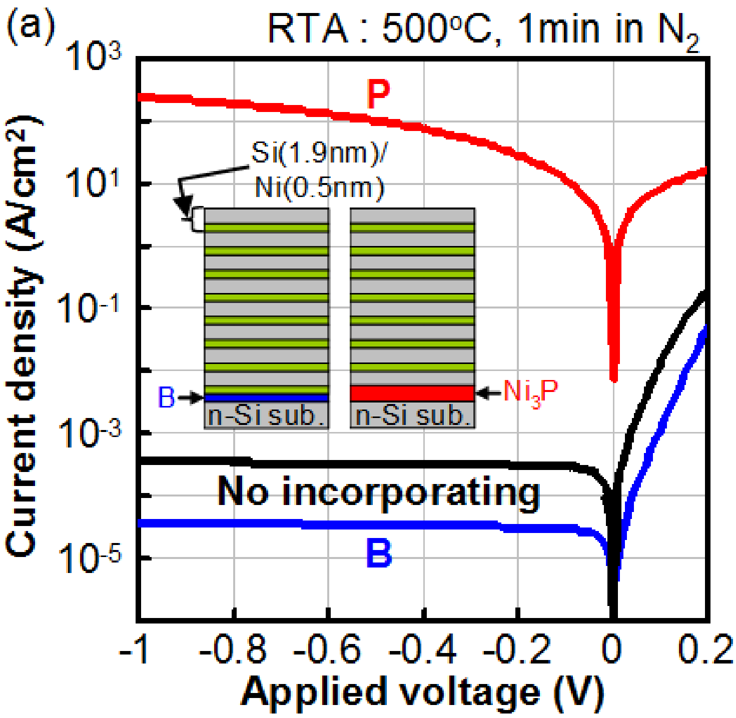


Fig 1-7 Image of obtaining $NiSi_2$ from Ni and Si stack structure



Y. tamura et al, Abstract #2663, Honolulu PRiME 2012

Fig 1-8 J-V characteristics of Schottky diode which was contacted $NiSi_2$ and n-type Si substrate

1.7 Purpose of this study

In n-type diamond, there is high Schottky barrier height cause of pinning effect and it is difficult to achieve low contact resistance. In this study, the major purpose is realizing that low contact resistance and ohmic contact. As an approach for this, modulate Schottoky barrier height by inserting dopant materials to interface in Si. This issue is considered the same thing as possible and to reduce contact resistance in diamond.

The purpose of the study is investigation of the effect on contact when phosphorous is put at the interface of n-type diamond.

Chapter 2

Fabrication and Characterization Method

2.1 Experimental procedure

Diamond substrates used in this work include heavily phosphorus-doped *n*-type epitaxial layer at the surface with concentration of 8×10^{19} cm^{-3} and over 10^{20} cm^{-3} grown on synthetic Ib diamond substrate [3]. Fig 2-1 shows process flow of this study. The substrates were cleaned in two steps. One is H_2SO_4 and H_2O_2 mixed acid solution at 140 ^{o}C for 10 min. The other is H_2SO_4 and HNO_3 mixed acid solution about 200 ^{o}C for 15 min. RF sputtering method was used to deposit metals and gates were patterned using lift-off method. Annealing was performed in N_2 gas ambient from 400 ^{o}C to 900 ^{o}C for 1 min.

- **n^+ Diamond substrate**
  Phosphorus-doped Concentration : (1)8.0×10^{19} cm^{-3}
  (2)Over 10^{20} cm^{-3}
- **H_2SO_4 and H_2O_2 acid cleaning 10min**
- **H_2SO_4 and HNO_3 mixed acid cleaning 10min**
- **Photoresist coating and photolithography**
- **Metal deposition by RF sputtering**
  (Ti, TiC, Ni, NiSi2, Ni3P)
- **Transmission Line Model (TLM) Electrodes Patterning by liftoff process**
- **Annealing in N_2 atmosphere at 400~900^{o}C**
- **Measure current–voltage characteristics and calculate contact resistances**

Fig 2-1 process flow of diamond contact

2.2 Experimental details and principle

2.2.1 Diamond substrate

This study used diamond substrate which doped Phosphorus. The diamond substrates are fabricated by National Institute of Advanced Industrial Science and Technology. Phosphorus doped diamond film was grown on the synthetic Ib diamond substrate made by HPHT (High Pressure High Temperature) method. The film thickness is 1.1 μm, crystal orientation is (111) and size is 2 x 2 mm. Carbon source of CVD was CH_4 and Phosphorus source was PH_3. [13–15]

Two samples with different concentrations. Doping concentrations were 8×10^{19} and over 10^{20} cm^{-3}. Fig 2-2 shows schematic image of diamond substrate in used this study. Fig 2-3 shows AFM image of diamond substrate (concentration over 10^{20} cm^{-3}).

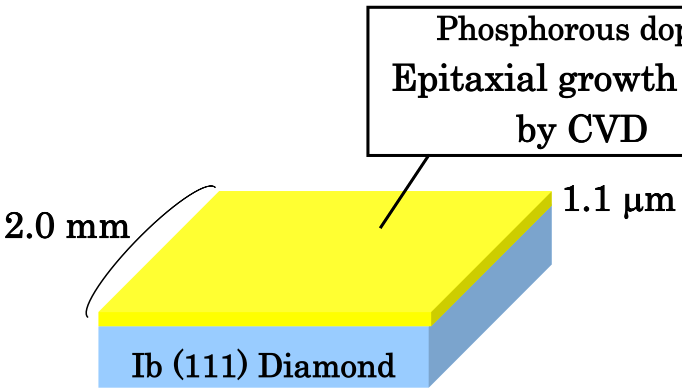


Fig 2-2 Diamond substrate of this study

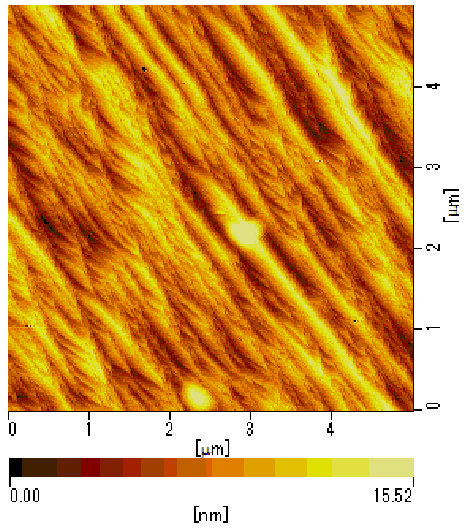


Fig 2-3 AFM image of diamond substrate

2.2.2 Structures of electrode

There were six structures of electrodes in this work. Figs 2-3 and 2-4 show schematic structures.

Fig 2-5 (a) and (b) were a simple Ni and Ni_3P layer of 20 nm thick as a control. Fig 2-5 (c) is a Ni and Si multi-stacking structure to form $NiSi_2$ by annealing. In this process, it is possible to control the composition easily by changing the layer thicknesses during stacking. Ni and Si films with thicknesses of 0.5 and 1.9 nm, respectively, were cyclically sputter deposited on substrates for 32 repetitions. These thicknesses were set to atomic ratio of Ni and Si 2 : 1. In the sample (d), the bottom layer was changed to Ni_3P, The Ni_3P layer thickness was 0.7 nm grown by the sputter deposition. The use of Ni_3P bottom layer was expected that Phosphorous is diffused into the diamond surface region and reduce contact resistance.

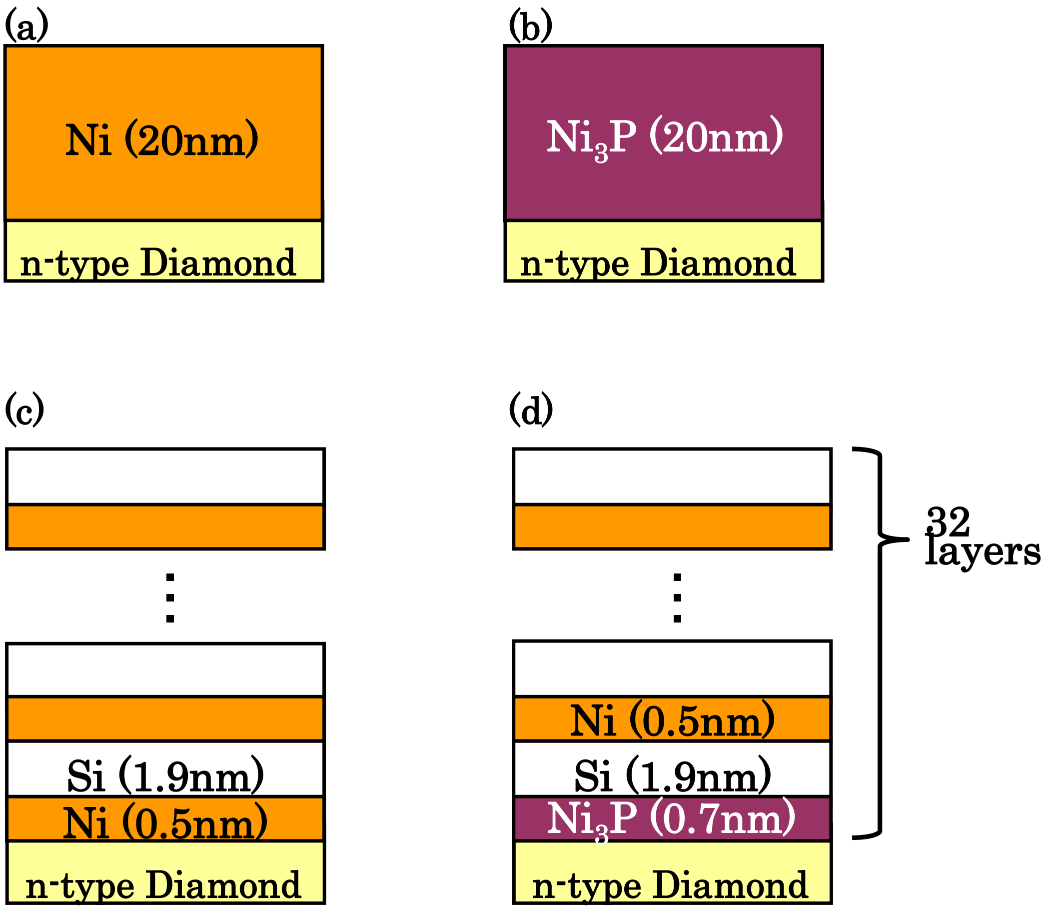


Fig 2-4 Structures of electrode using Ni

2.2.3 Substrate treatment

The diamond substrate treatment of the first step, which use a solution of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) ($H_2SO_4 : H_2O_2 = 4 : 1$), was performed to remove any organic material and metallic impurities. After dipping in the chemicals to clean the substrate, the clean wafer was dipped in DI (De Ionize) water to rinse away the chemicals. The process dipping the wafer in DI water after dipping the wafer in chemicals with each cycle is important.

Next substrate treatment, which use a solution of sulfuric acid (H_2SO_4) and nitric acid (HNO_3) ($H_2SO_4 : HNO_3 = 4 : 1$), was performed oxidation and roughening of diamond surfaces occur simultaneously. [16] The wet-oxidation treatment transforms the diamond surface from one terminated by a full monolayer of hydrogen to one terminated by oxygen, OH, and so on. The electrochemical properties of diamond electrodes were sensitive to the surface termination. The oxygen-terminated diamond electrode has significantly different properties in the electrochemical environment.

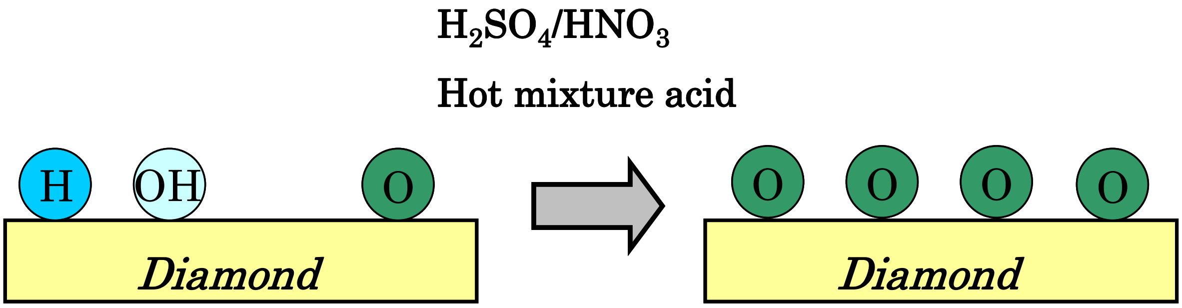


Fig 2-6 Change the termination on diamond surface

2.2.4 Photolithography

Photolithography (or "optical lithography") is a process used in microfabrication to selectively remove parts of a thin film or the bulk of a substrate. It uses light to transfer a geometric pattern from a photomask to a light-sensitive chemical "photoresist", or simply "resist," on the substrate. A series of chemical treatments then either engraves the exposure pattern into, or enables deposition of a new material in the desired pattern upon, the material underneath the photo resist. It is used because it can create extremely small patterns (down to a few tens of nanometers in size), it affords exact control over the shape and size of the objects it creates.

In case of this study, photolithography was used for the method to make pattern of electrodes. The apparatus is MJB4 of Karl Süss contact-type mask aligner. At first, the substrates were coated with thicker or thiner positive type photoresists by spin-coating method. Secondly, the coated photoresists were baked at 115 ^{o}C for over 5 min by using electrical hotplate. Then, spin-coated photoresist layers were exposed through e-beam patterned hard-mask with high-intensity ultraviolet (UV) light with the wavelength of 405 nm. The exposure duration was set to 4 sec and 10 sec for thinner photoresist and thicker one, respectively. Thirdly, exposed wafers were developed using the specified tetra-methyl-ammonium-hydroxide (TMAH) developer called NMD-3 (Tokyo Ohka Co. Ltd.). The wafers were dipped into the solvent for 1 to 2 minute.

1. Photoresist (S1805) spin-coating by 4000 rpm
2. Baking at 115 °C for over 5 min.
3. Exposure 4 sec without mask
4. Photoresist (S1818) spin-coating by 4000 rpm
5. Exposure 10 sec with mask
6. Development (NMD3)

Fig 2- The process flow of photolithography

Figure 2-3 The photo of photolithography apparatus

2.2.5 RF magnetron-sputtering

After Photolithography, metal films were deposited by radio frequency (RF) magnetron sputtering.

Sputtering is one of the vacuum processes used to deposit ultra thin films on substrates. A high voltage across a low-pressure gas (usually argon at about 10 mTorr) is applied to create a "plasma," which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike the "target," composed of the desired coating material, and cause atoms of the target to be ejected with enough energy to travel to the substrate surface. RF magnetron-sputtering system shown in Fig 2-7.

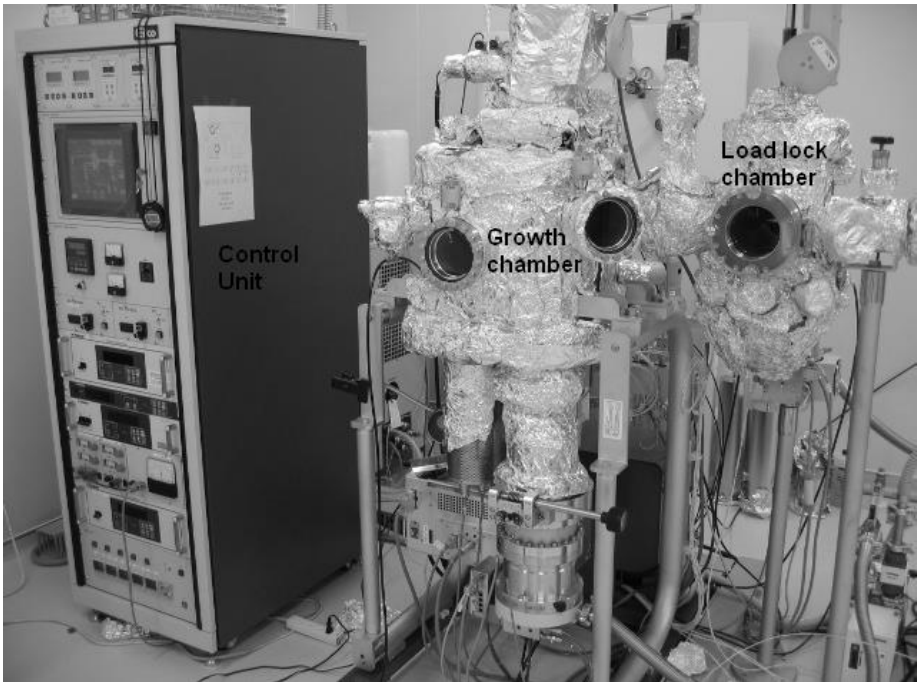


Figure 2-4 Photo of UHV Multi Target Sputtering System ES-350SU

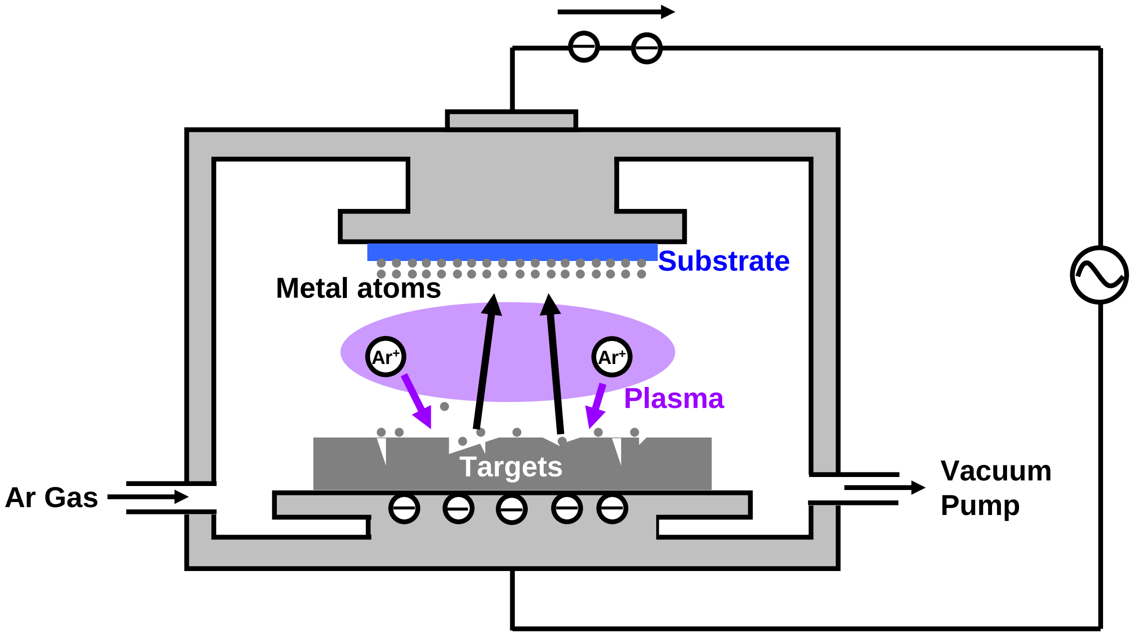


Fig 2-7 Schematic internal structure of RF sputtering system.

2.2.6 Lift off

Lift-off method is simpler process than dry etching. Lift off process fist step is making phororesist pattern on the substrate such a Fig2-8 (1).The second step is Metal deposit by RF magnetron-sputtering and so on. Finally, the substrate immersed in acetone portion was peeled off to form a pattern with metal. In this method, depositing a metal film must be room temperature. Because substrate becomes hot, there is a possibility that the resist pattern is deformed.

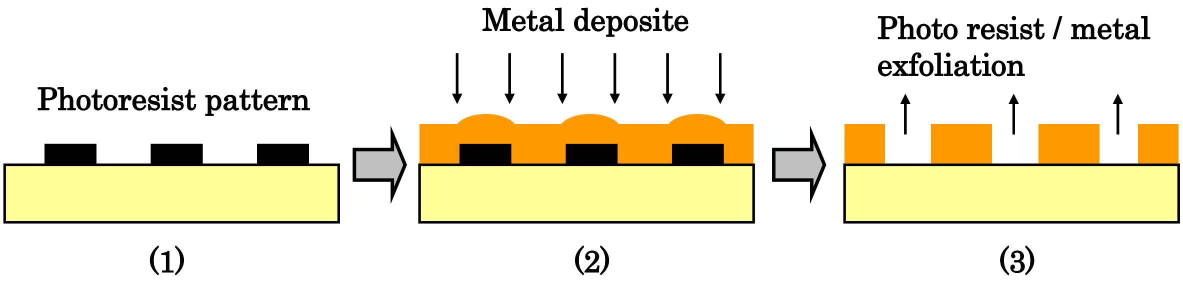


Fig 2-8 The state of the lift-off

2.2.7 Thermal Annealing Process

Thermal annealing was used electrode and interface formation. In this study, low temperature (between 400°C-900°C) thermal treatments utilizing infrared lamp typed rapid thermal annealing (RTA) system were used. The ambience in furnace was vacuumed adequately prior to every annealing cycle and then N_2 gas was provided with flow rate of 1.5 l/min while preserving the furnace pressure at atmospheric pressure. All annealed samples were removed from the chamber under 100 °C

2.3 Measurement methods

2.3.1 J-V (Leakage Current Density – Voltage) Measurement

To estimate the current density, *I-V* characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard.) and current divided by the electrode area.

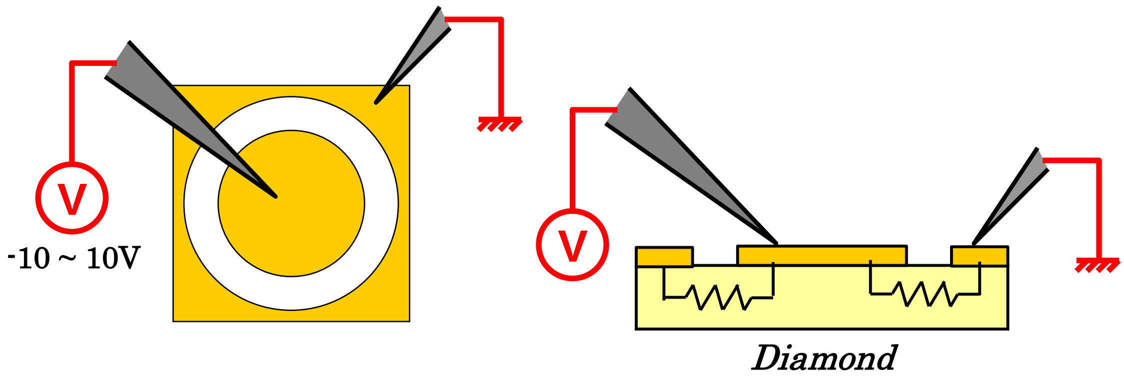


Fig 2-9 Image of the J-V measurement

2.3.2 Transmission Line Model (TLM)

Performance index of the ohmic contact is expressed in contact resistance (ρc). The contact resistance can be written as

$$\rho_c \equiv \left(\frac{\delta V}{\delta I} \right)_{V=0} (\Omega \cdot cm^2) \qquad \text{(2-1)}$$

TLM method is often used to measure the contact resistance. [17–19] TLM method is considered as equivalent to the transmission line circuit electrode and the semiconductor layer below. The form of the electrodes are circular or rectangular generally used. In the method for measuring the resistance of the rectangle electrode, current can affect the results of the resistance measurement at the electrode edge. It is necessary mesa structure to remove the edge current. Process is complicated for that. However, the edge is not affected if circular pattern used, It is able to be more accurate analysis.

In this work used circular electrodes as shown Fig 2-10 were used. a_2 - a_1 is space d.

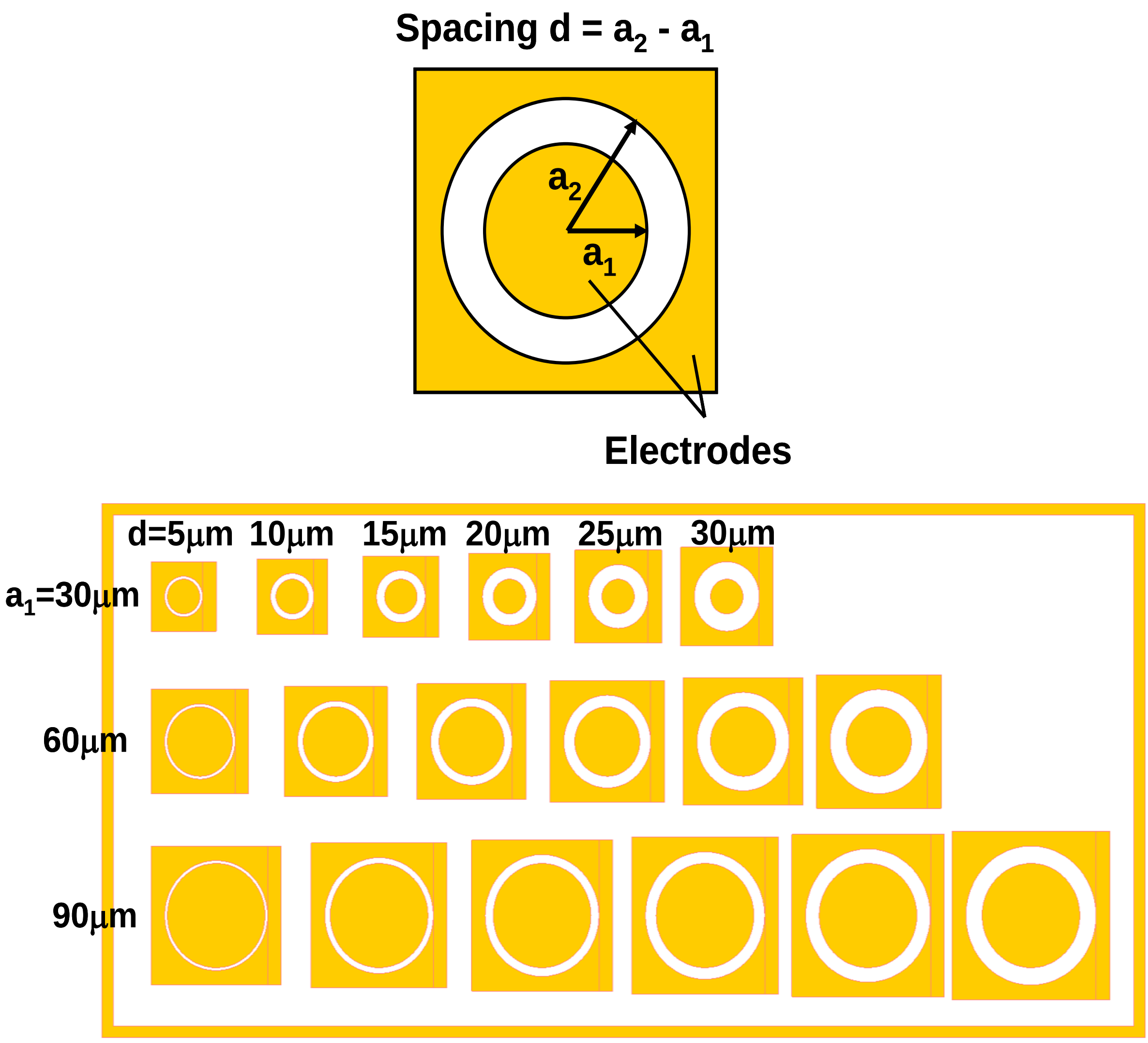


Figure 2-9 Electrode pattern of c-TLM using this study

The first step is measuring the characteristics between the outer and inner electrodes. The second step is calculating the resistance using Ohm's law from the IV characteristics. The gap area which is between electrodes can be written as

$$S = \pi(a_2^2 - a_1^2) = \pi(a_2 + a_1)(a_2 - a_1) = \pi(a_2 - a_1) \cdot d \qquad (2\text{-}2)$$

Thus the area is proportional to d. Propagation length can be determined by linear approximation of the characteristic R-d as shown Fig2-10 . There are so $-2Lt$ in the d-axis intercept where the line extrapolated to the zero resistance.

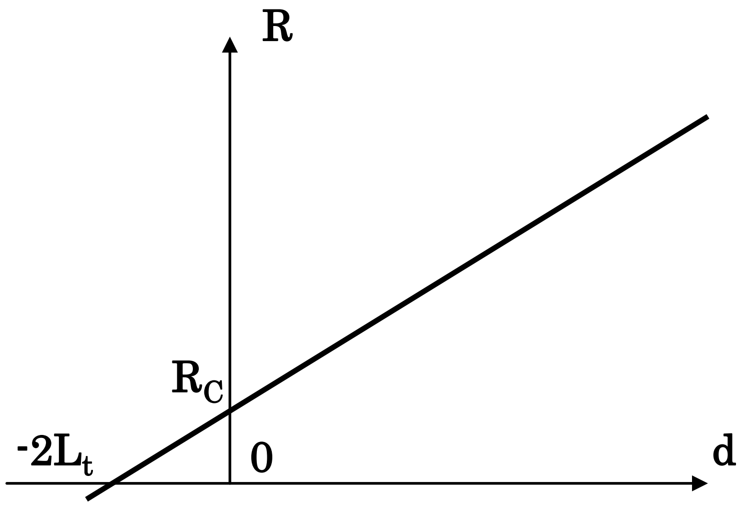


Fig 2-10 R-d characteristics image

When it is a_2, $a_1 >> L_t$, Resistance R which is measured is written as

$$R = \left(\frac{R_{SK} \cdot L_t}{2\pi a_2} + \frac{R_{SK} \cdot L_t}{2\pi a_1} \right) + \left(\frac{R_{SH} \cdot \ln\left(\frac{a_2}{a_1} \right)}{2\pi} \right) \qquad (2\text{-}3)$$

First and second terms of the right side of this equation represent the resistance of the semiconductor layer under the electrode. This indicates that resistance is inversely proportional to the circumference, is proportional to the propagation length in the case of c-TLM. The third term represents the resistance of the semiconductor layer other than the electrode immediately below. It is expressed as the resistance of expression (2-3) is determined by measuring the sum of the resistance which were under electrode and the other. Assume $R_{SH} = R_{SK}$, and organize the expression (2-3),

$$R = \frac{R_{SH}}{2\pi} \left[L_t \left(\frac{1}{a_2} + \frac{1}{a_1} \right) + \ln\left(\frac{a_2}{a_1} \right) \right] \qquad (2\text{-}4)$$

ΔV the voltage drop between the electrodes, and the current value I. Ohm's law and the equation (2-4),

$$\Delta V = \frac{I \cdot R_{SH}}{2\pi} \left[L_t \left(\frac{1}{a_2} + \frac{1}{a_1} \right) + \ln\left(\frac{a_2}{a_1} \right) \right] \qquad (2\text{-}5)$$

Sheet resistance is obtained from this equation.

Since the sheet resistance is obtained and the propagation length I can be obtained from

$$\rho_c = R_{SH} \cdot L_t^2 \qquad (2\text{-}6)$$

the contact resistance.

Chapter 3

Electrical characteristics and contact resistance of phosphorus doped diamond

3.1 Introduction

In this study, we investigated *J*-*V* characteristics and the analysis of Ni, Ni_3P, and stacked structure $NiSi_2$ electrodes/n^{+}-diamond samples. Fig 3-1 shows schematic image of measurement. Using electrode in this chapter is inside electrode radius 90μm and gap d 30μm. The measurement was performed by applying -10 ~ 10 V to the internal electrode. *J*-*V* characteristics were measured at various annealing temperatures ranging from 400 °C to 900 °C and the analysis is natural logarithm reverse diode current density and differential ln|J|.

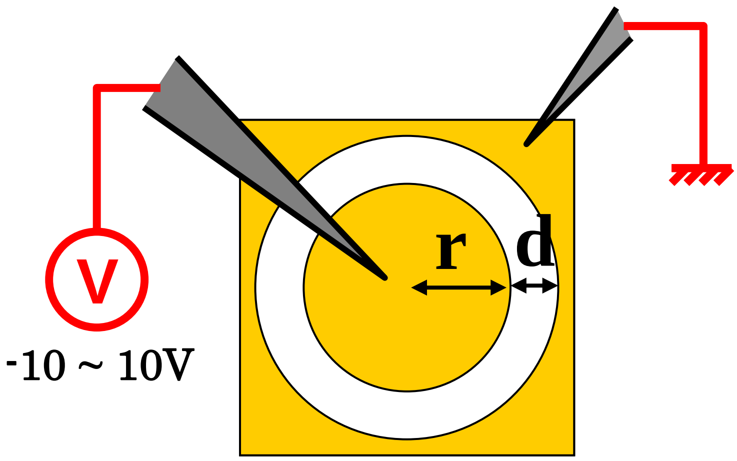


Fig 3-1 Image of measurement

3.2 Electrical characteristics of Ni, Ni_3P and $NiSi_2$ electrodes

3.2.1 $NiSi_2$ electrodes on diamond substrate doped 10^{19} cm^{-3}

Fig 3-2 shows J-V characteristics of $NiSi_2$ electrode on 10^{19} cm^{-3} doped n-type diamond substrate. (a) is natural logarithm current density and (b) is differential (a). Annealing temperatures were 400-900 °C. The contact behavior didn't become ohmic. In 825 °C annealing, current density is increased compared with as deposited in the low bias region (1~2 V). But applying at 2~10 V, the as deposited sample exhibited the largest current density. It indicates that there is different conduction mechanism at low and high bias regime. When annealing over 850 °C current density is reduced. This reason is the aggregation of the $NiSi_2$ electrode. In the (b), it can be seen that the behavior can be classified into two groups. This indicates there is two kinds of conduction that changes at from 700 to 825 °C.

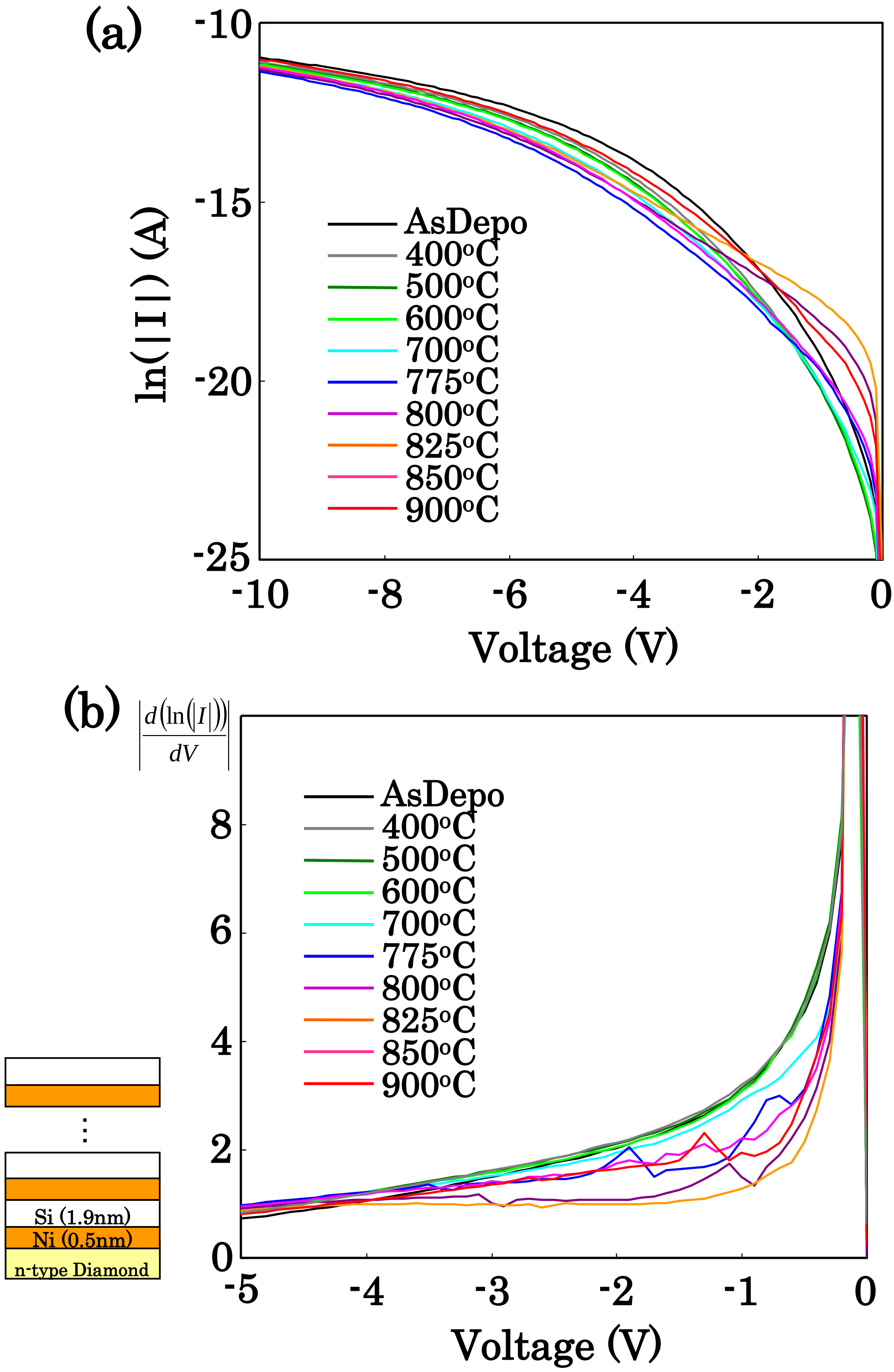


Fig 3-2 characteristics of $NiSi_2$ electrodes at several annealing temperature on 10^{19} cm^{-3} concentration substrate (a) ln|J|-V characteristics (b) Differentiating ln|J| characteristics

3.2.2 P putted $NiSi_2$ electrodes on diamond substrate doped 10^{19} cm^{-3}

Fig 3-3 shows J-V characteristics of $NiSi_2$ electrode on 10^{19} cm^{-3} doped n-type diamond substrate. (a) is natural logarithm current density and (b) is its differential (a). Annealing temperatures were 400-900 ^{o}C. The contact behavior didn't become ohmic. In 850 ^{o}C annealing, current density is increased compared with as deposited in the low bias region (1~2 V) and in high bias region also the highest. The current density has increased especially in the low bias compared with that only $NiSi_2$ electrode. It indicates that there is different conduction low and high bias. When annealing over 900 ^{o}C current density is reduced. This reason is aggregation of the $NiSi_2$ electrode. In the (b), it can be seen that the behavior can be classified into two groups. This indicates there is two kinds of conduction that change from 700 to 850 ^{o}C.

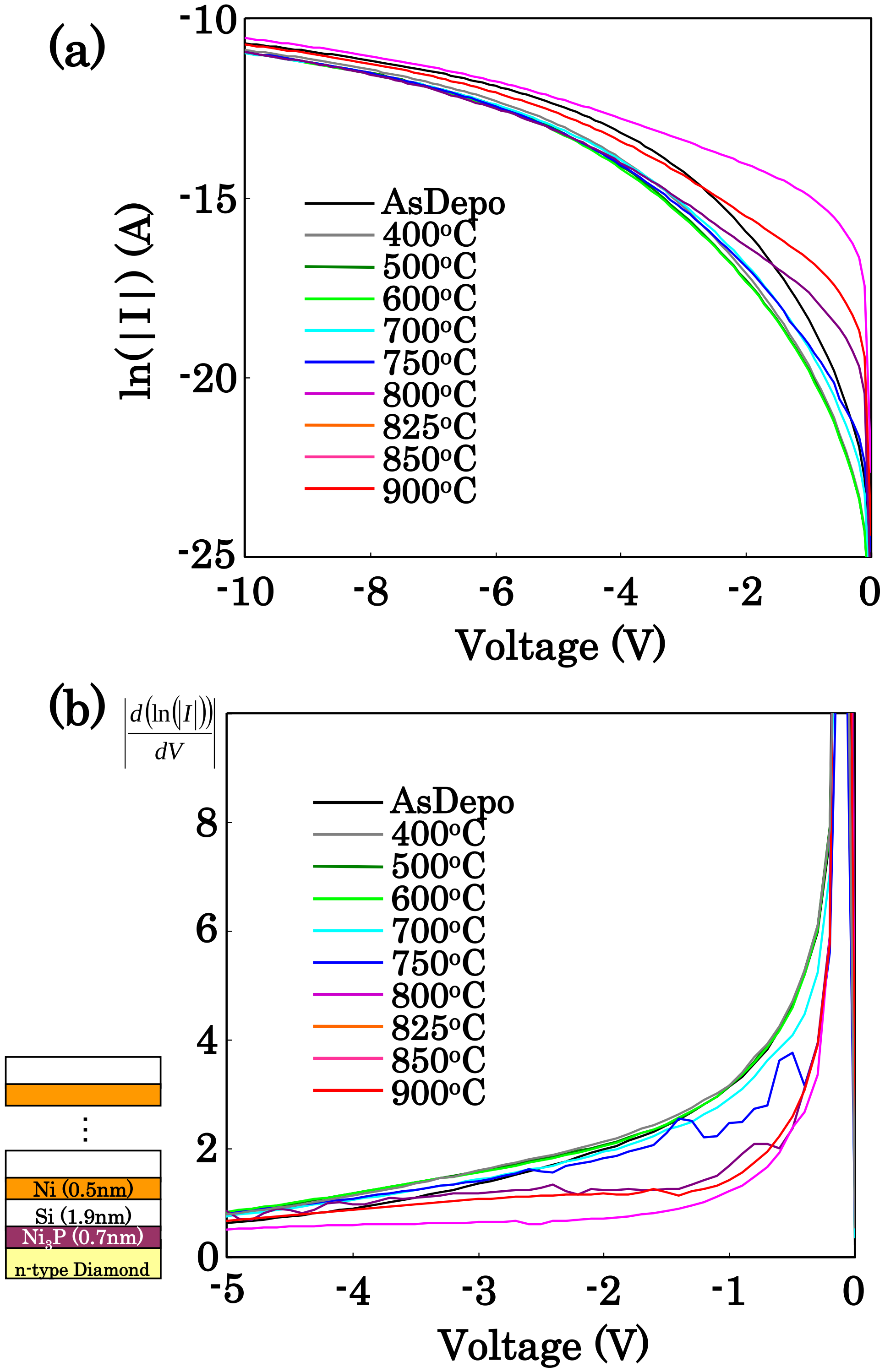
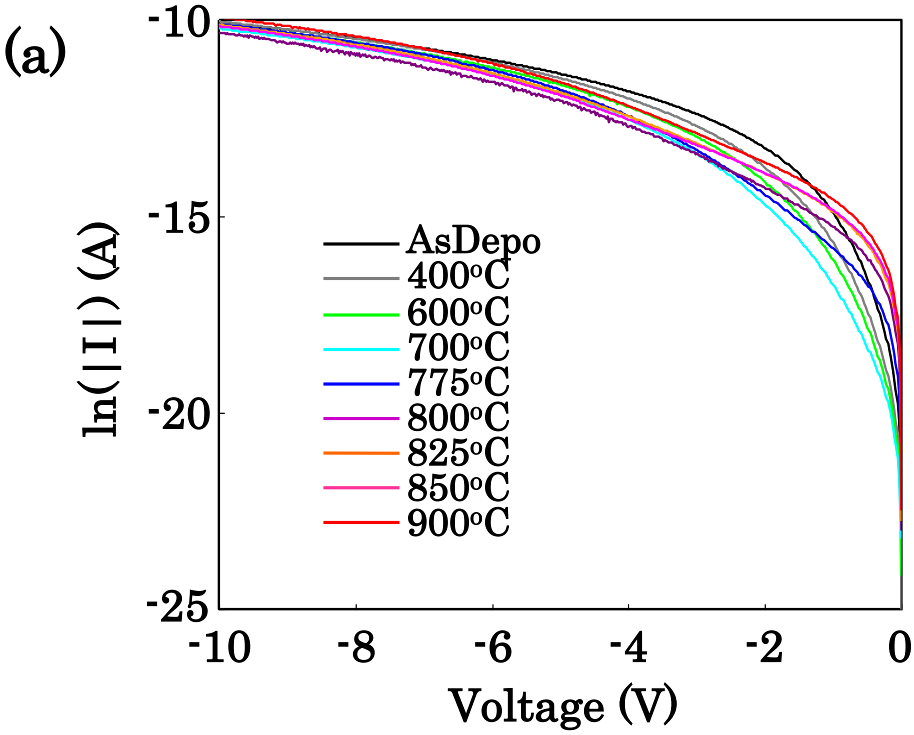


Fig 3-3 characteristics of P intercalated $NiSi_2$ electrodes at several annealing temperature on 10^{19} cm^{-3} concentration substrate (a) ln|J|-V characteristics (b) Differentiating ln|J| characteristics

3.2.3 P intercalated $NiSi_2$ electrodes on diamond substrate doped 10^{20} cm^{-3}

Fig 3-4 shows J-V characteristics of $NiSi_2$ electrode on 10^{20} cm^{-3} doped n-type diamond substrate. The substrate was doped ne order of magnitude higher concentration than the other substrate. (a) is natural logarithm current density and (b) is its differential (a). Annealing temperatures were 400-900 ^{o}C. The contact behavior didn't become ohmic. In 900 ^{o}C annealing, current density is increased compared with as deposited in the low bias region (1~2 V). But applied 2~10 V, as deposited has the largest current density. It indicates that there is different conduction low and high bias. In the (b), it can be seen that the behavior can be classified into two groups. This indicates there is two kinds of conduction that change from 700 to 825 ^{o}C.



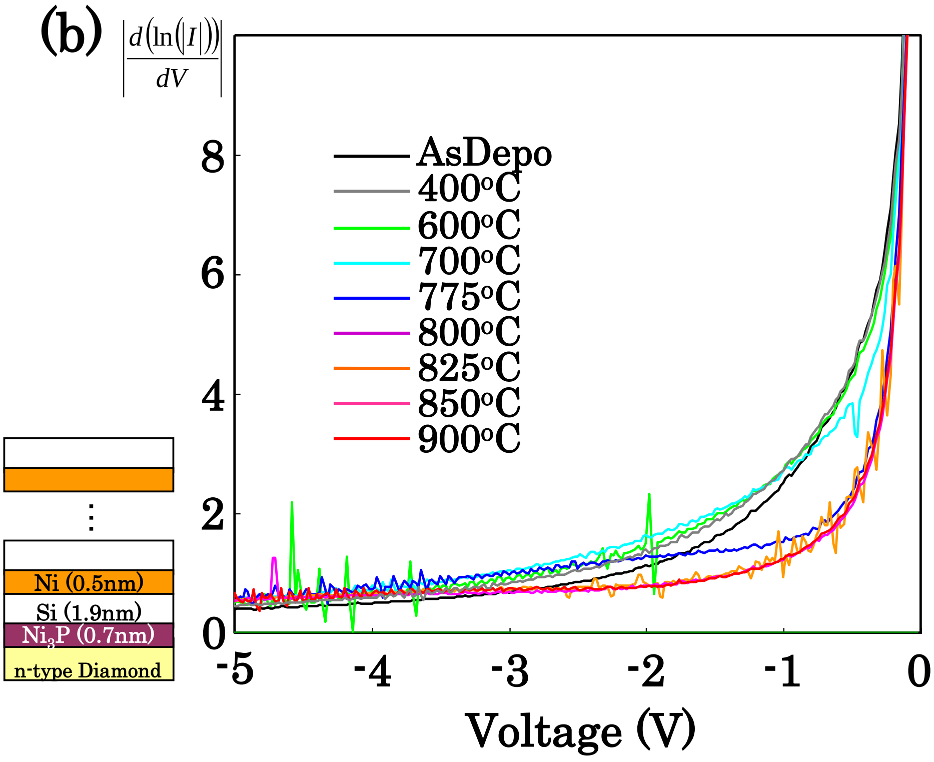


Fig 3-4 characteristics of P intercalated $NiSi_2$ electrodes at several annealing temperature on 10^{20} cm^{-3} concentration substrate (a) ln|J|-V characteristics (b) Differentiating ln|J| characteristics

3.2.4 Ni_3P electrodes on diamond substrate doped 10^{19} cm^{-3}

Fig 3-5 shows J-V characteristics of $NiSi_2$ electrode on 10^{19} cm^{-3} doped n-type diamond substrate. (a) is natural logarithm current density and (b) is its differential (a). Annealing temperatures were 400-900 ^oC. The contact behavior didn't become ohmic. With the annealing, the current increases. The current is increased in most 900 degrees. Symptom low bias current flows, as well NiSi2 was not observed.

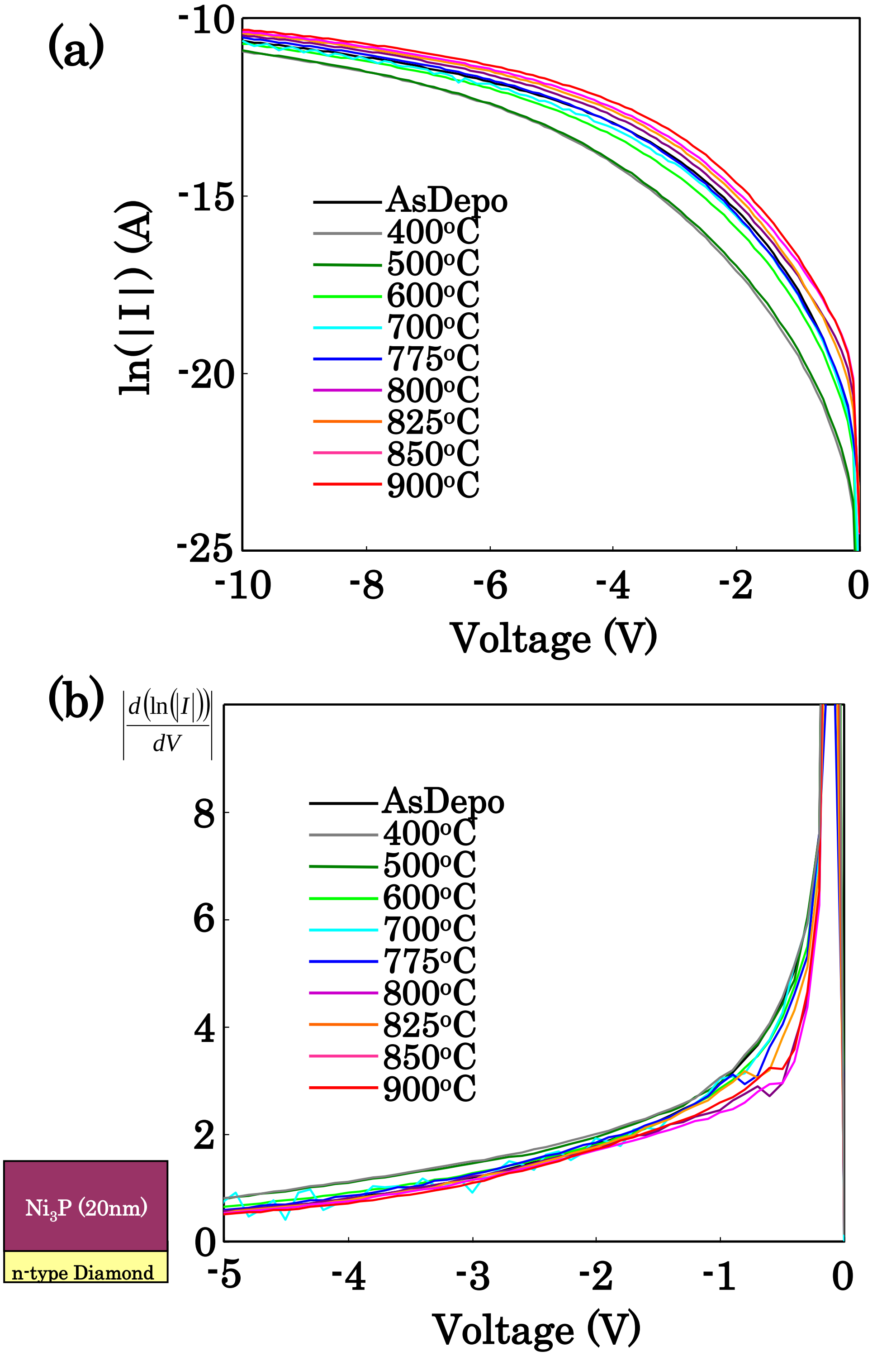


Fig 3-5 characteristics of Ni_3P electrodes at several annealing temperature on 10^{19} cm^{-3} concentration substrate (a) ln|J|-V characteristics (b) Differentiating ln|J| characteristics

3.3 The reason of change J-V characteristics Model

3.3.1 The Case of NiSi2 only

Hopping conduction has been considered most dominant conduction. Fig 3-6 (a) shows image of hopping conduction and (b) shows hopping conduction relationship between the energy. In hopping conduction, carriers move between doped levels by tunneling. Hopping conduction current can write as

$$J_H = 2ena\mu E \exp\left(-\frac{U}{kT}\right)\sinh\left(\frac{eEa}{2kT}\right) \quad (\mathrm{A/cm^2}) \qquad (3\text{-}1)$$

When distance between donors shrinks; donor density increase, tunneling probability and hopping conduction grow.

Fig 3-7 shows the Carbon solubility to Silicon.[19] C_s represents substitution solubility and C_i represents intrusion. In diffusion of carbon to silicon, substitution diffusion is dominant. Carbon diffuses to silicon over 700 ^{o}C annealing. Fig 3-8 shows the model image of changing close interface. When diamond is annealed over 700 ^{o}C, carbon diffuses from diamond to $NiSi_2$ and SiC is formed. Because of this reason, Phosphorous is left near the diamond interface. Fig 3-9 shows interfacial band diagrams at the n-diamond/metal interface. Phosphorous that are left makes high concentration layer. High concentration layer facilitates the hopping conduction. To facilitate this, hopping conduction is possible from low bias and low bias current increases.

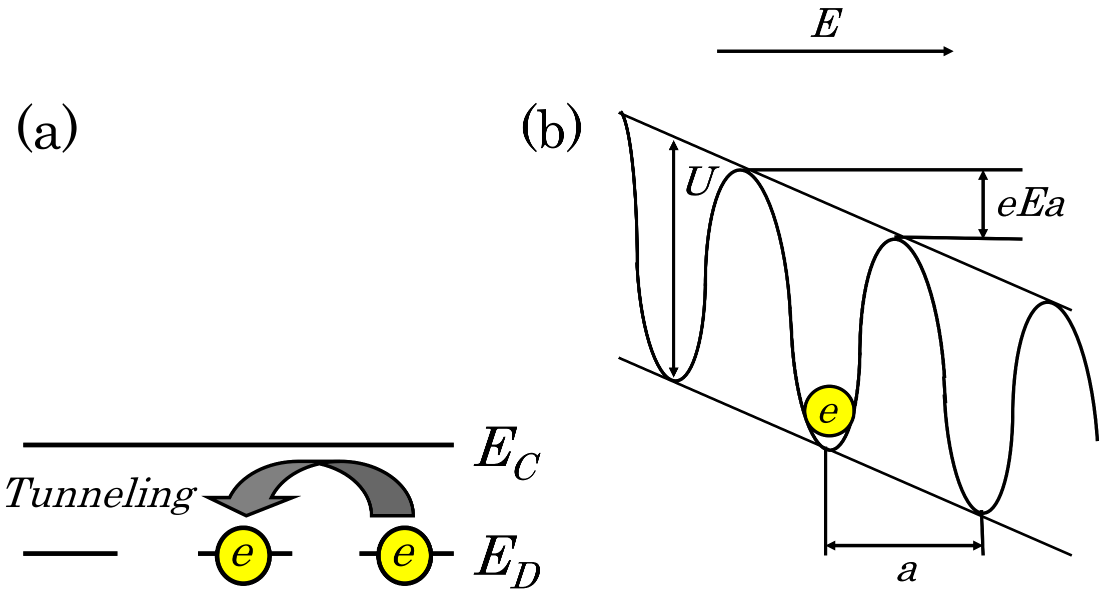


Fig 3-6 (a) Image of hopping conduction (b) Hopping conduction relationship between the energy.

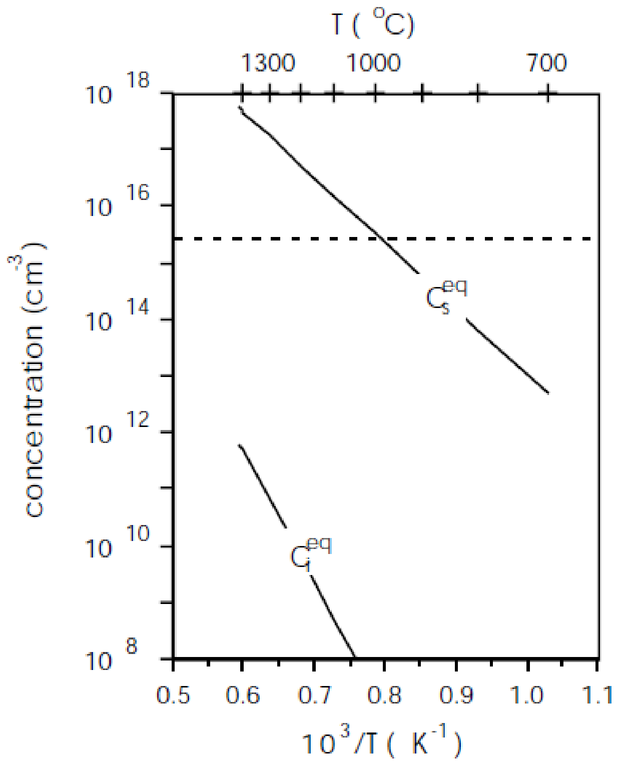


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Fig 3-7 Carbon solubility to Silicon

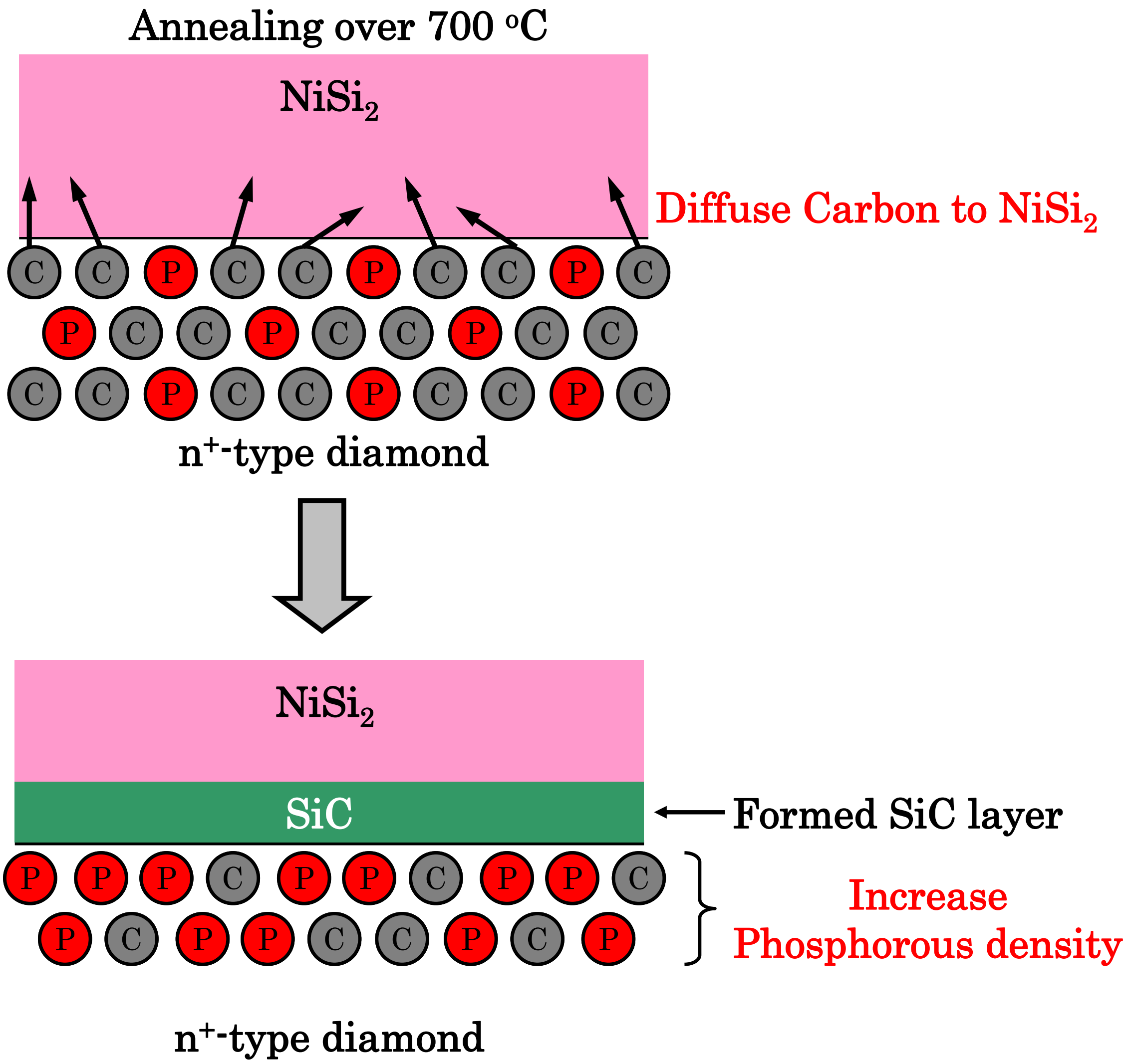

Fig 3-8 The model image of changing close interface

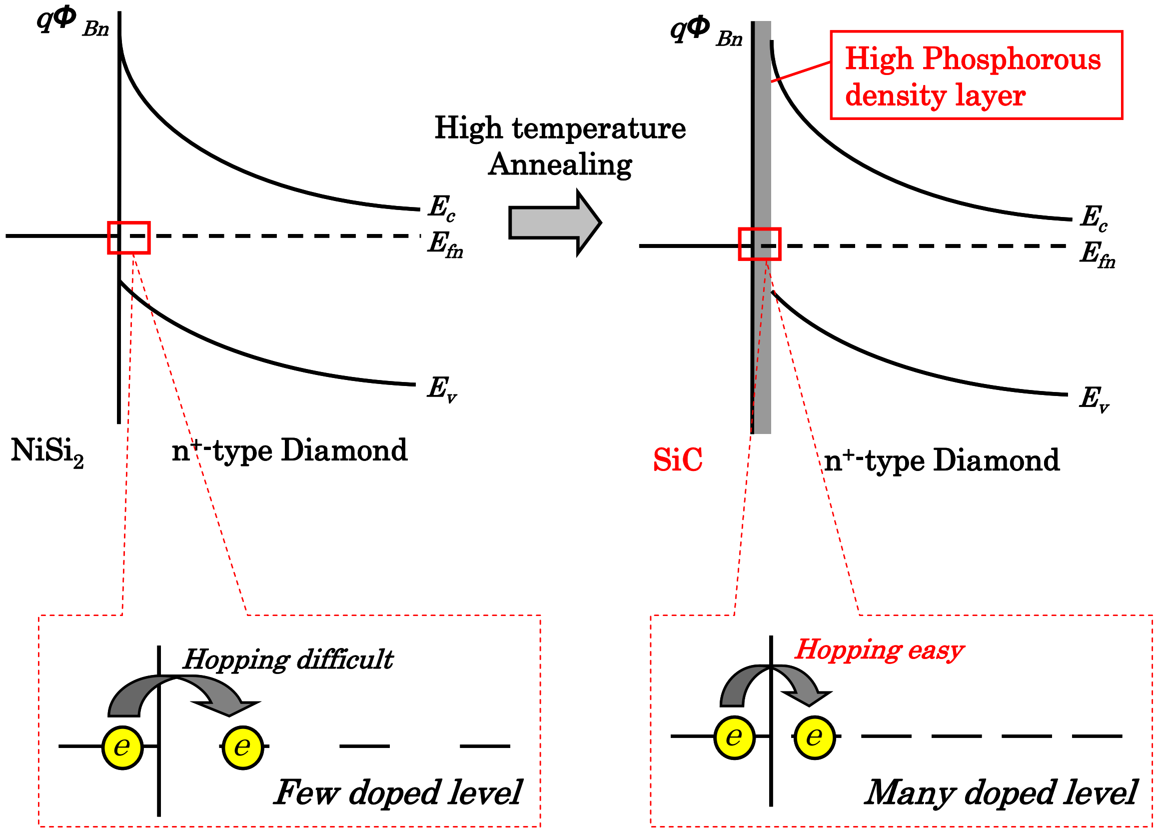

Fig 3-9 Interfacial band diagrams at the n-diamond/metal interface

Fig 3-10 shows Raman spectra of DLC with several anneal temperature. (a) is only DLC film. (b) is DLC film covered Ni 1nm. There is G-band peak from 1550 to 1650 cm^{-1}. G-band is expressed sp^2 bond, broad peak is expressed amorphous structure, peak shift is expressed larger cluster size and G-band peak sharpened is expressed close only sp2 bond. (b) indicate cutting sp^3 bond and sp^2 bond made by Ni working as catalyst. Therefore in case of diamond substrate, there is a possibility that Ni as catalyst cuts sp^3 bond of diamond and facilitates carbon diffusion.

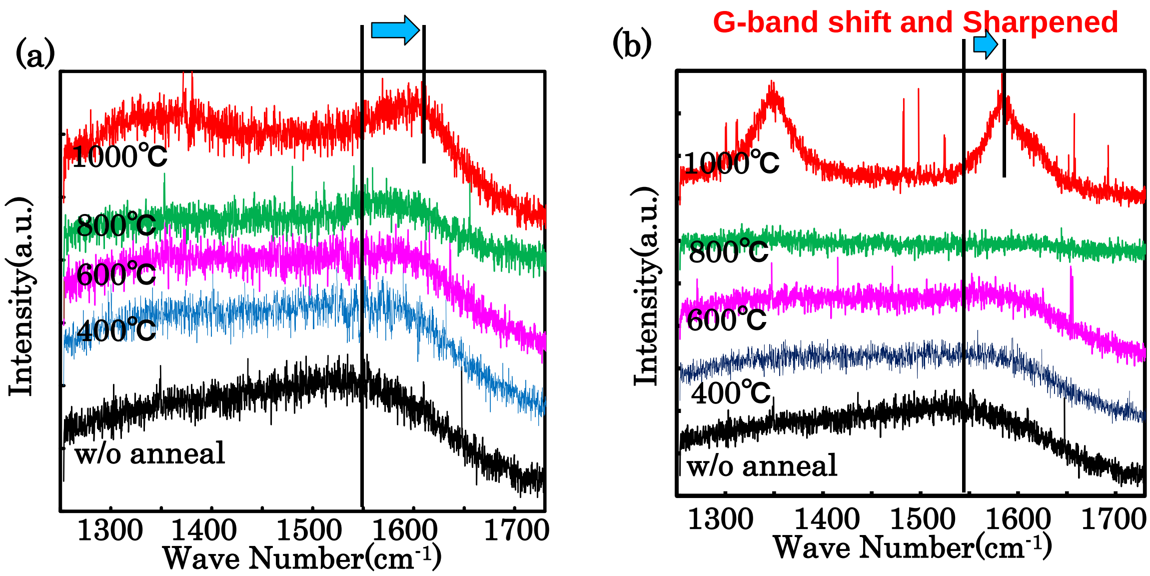

Fig 3-10 Raman spectra of DLC with several anneal temperature (a) only DLC film (b) Ni film on DLC

3.3.1 The Case of Phosphorous in electrodes

In case of Phosphorous incorporated $NiSi_2$ there is P electrode side different from only $NiSi_2$ electrode. P in the electrode can affect Schottky barrier such as Fig 3-4 Ni_3P electrode J-V characteristics. P can change Schottky barrier height or depletion layer thickness because conduction wasn't changed in Ni_3P electrode. Compared J-V characteristics of NiSi2 electrodes with and without P, J-V behavior has not changed. Therefore it is possible that P enter the diamond and P concentration of diamond surface is higher than NiSi2 without P electrode.

Conclusion

One of the issues for diamond electron devices is high contact resistance at the metal and diamond interface. Small contact resistance is an important factor to fabricate high-performance and low-loss devices. *n*-type ohmic contact with small contact resistance has not been realized yet, despite various efforts have been done and the current minimum value of contact resistance is 2.2×10^{-3} Ω•cm^2 by using Au/Pt/Ti electrode. The reasons of high contact resistance of *n*-type diamond are large Schottky barrier height (4.6 eV) and Fermi level pinning. In Si Schottky diode, barrier height can be controlled by putting dopant materials (P or B) at diamond and metal electrode interface. In this thesis, a novel method to reduce the contact resistance has been proposed by incorporating phosphorus atoms at the interface.

Diamond substrates used in this work include heavily phosphorus-doped *n*-type epitaxial layer at the surface with concentration of 8×10^{19} and over 10^{20} cm^{-3} grown on synthetic Ib diamond substrate. Electrode is a nickel and silicon multi-stacking structure to form $NiSi_2$ by annealing. In this study, Ni and Si films with thicknesses of 0.5 and 1.9 nm, respectively, were cyclically sputter deposited on substrates for 32 repetitions. And the bottom layer was changed to Ni_3P, the Ni_3P layer thickness was 0.7 nm grown by the sputter deposition. The use of bottom layer was expected that Phosphorous is diffused into the diamond surface region and reduce contact.

An increase in reverse diode current has been observed he contact resistance is 7×10^{-2} Ω•cm^2 when P incorporated $NiSi_2$ electrodes have been annealed at 850 ^{o}C. The current is especially significantly increased at a low bias territory (1-2V) in comparison with Ti which is now commonly used as electrode. The reason for this is considered that interface of diamond and Si react to SiC and solid phase doping is occurred close at diamond surface. It has been shown that both Si and P atoms play an important role for effectively tuning the Schottky barrier height

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Yuki Tanaka