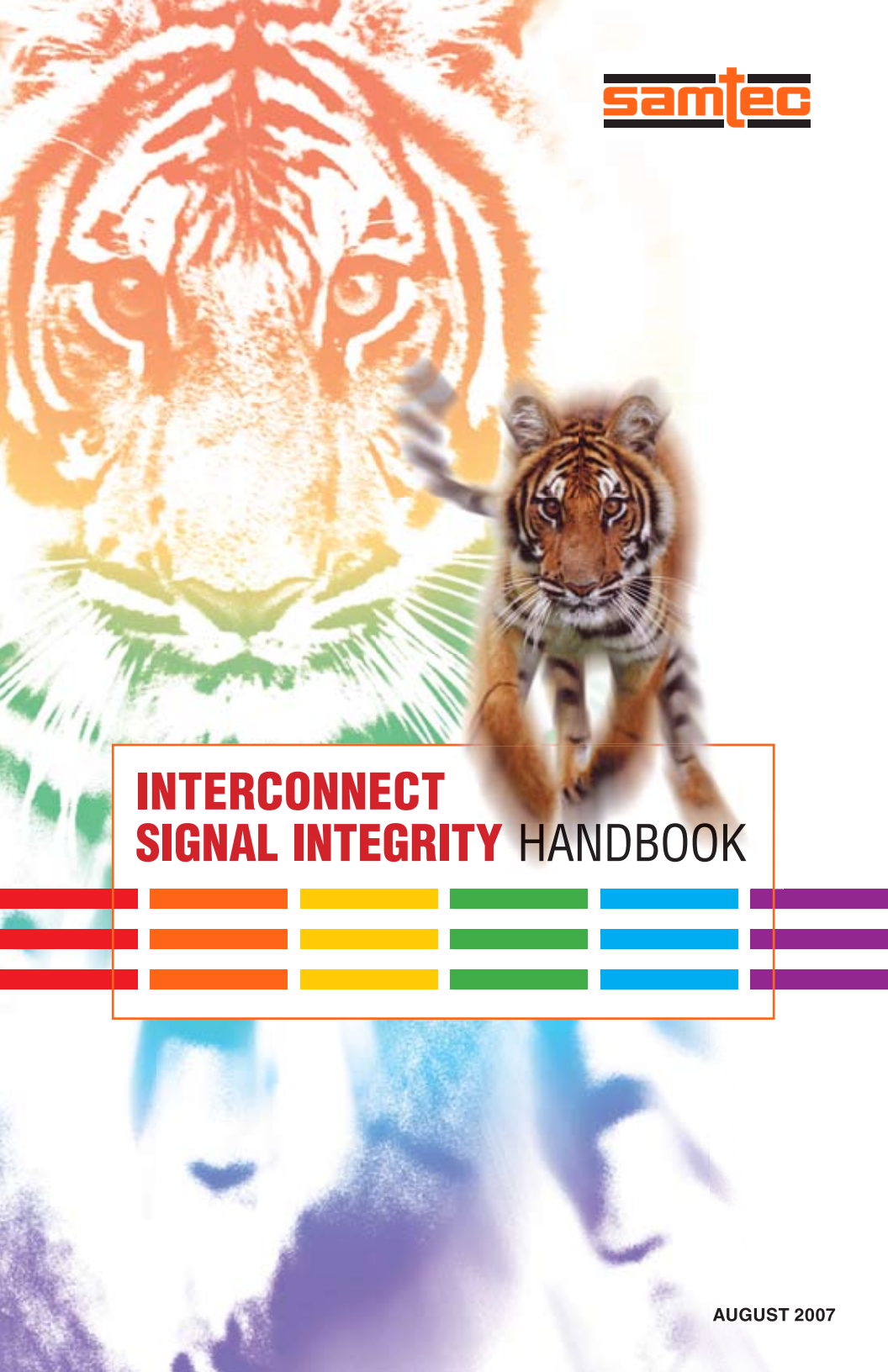

INTERCONNECT SIGNAL INTEGRITY HANDBOOK

AUGUST 2007

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Introduction

What is Signal Integrity?

Any time an electrical signal is transmitted, signal integrity is a concern. At its most basic level, signal integrity (SI) ensures that a signal is moved from "Point A" to "Point B" with sufficient quality or integrity to allow effective communication.

In a typical communication system, "Point A" is a signal transmitter, and "Point B" is a receiver. The signal transmission path connecting the two may be hard wired, such as a fiber or copper cabling system, or wireless, such as a cell phone network.

Signal integrity has been a concern in long distance communications for well over a century. More recently, SI has become a concern in shorter and shorter transmission paths. For example, in a modern system, the transmission path or interconnect between a computer motherboard and a daughter card attached to it can be a significant SI concern.

Interconnects can no longer be treated as an after-thought in the system design process. As rise times get shorter and clock frequencies faster, connectors and cables once considered electrically transparent can have a significant effect on a system's transmitted signal. Factors such as crosstalk, return loss, attenuation, and electromagnetic interference can all play significant rolls in determining what interconnect solution is optimal for a given application.

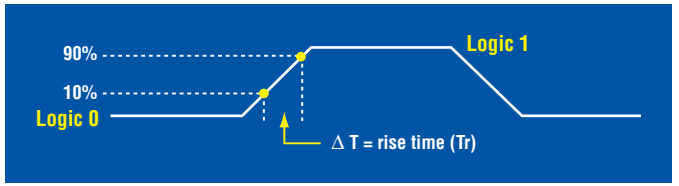
Providing a foundation for high speed decisions

The purpose of this handbook is to provide a reference for those with little or no Signal Integrity (SI) experience who are tasked with selecting a high speed interconnect, and to help enable them to make an informed decision when specifying components that will affect the Signal Integrity of their system.

Signal Integrity Fundamentals

WHEN DO I NEED A HIGH SPEED CONNECTOR?

The question "When do I need to use a high speed connector?" often arises. Unfortunately, with each application, the answer will vary. One rule of thumb is based on the signal edge rate, or rise time. Rise time is generally defined as the amount of time it takes for a signal to switch from one logic state to another. With rise times faster than about 1ns, many interconnects become a critical portion of the transmission path, and further analysis is often required.



Rise time

How do I know the connector will meet my needs?

Many methods are used to characterize and rate interconnect components. By understanding the basic electrical parameters, and how they are acquired and reported, valid comparisons can be made between various interconnects.

The -3dB insertion loss point is often viewed as a suitable "one number" bandwidth rating for passive interconnects. But further analysis of other electrical parameters most critical to a specific application may be warranted.

In some SI applications, a specific parameter may be critical to system performance even though the signal rise time may not be considered unusually fast. Such "clean signal" requirements might require low loss connections, extremely low crosstalk, or minimal reflections, and thus may still require an SI solution. Therefore, in some cases, additional high speed test data and circuit simulation models are required to provide enough information to choose an appropriate solution for a given high speed system.

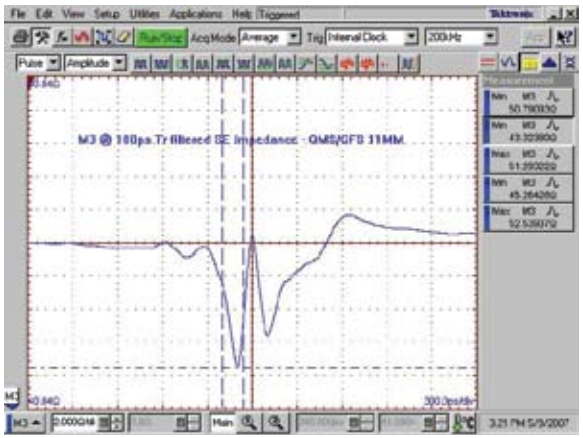
TIME DOMAIN VERSUS FREQUENCY DOMAIN

It is common for Signal Integrity Engineers to characterize component and system behaviors in two different environments or domains: time domain and frequency domain. This is mostly a matter of convenience and ease of use. Some phenomena are simply easier to understand and visualize in a particular domain. Because of test instrument capabilities, it may also be easier to characterize a component in one domain or the other. Similarly, one domain might offer more practical mathematical solutions to a certain type of problem.

Understanding Time Domain

The time domain describes the world as we normally see it. A data plot representing time domain behavior will use time as its horizontal axis. A particular characteristic of a component, such as a measured voltage or current, is plotted against the vertical axis.

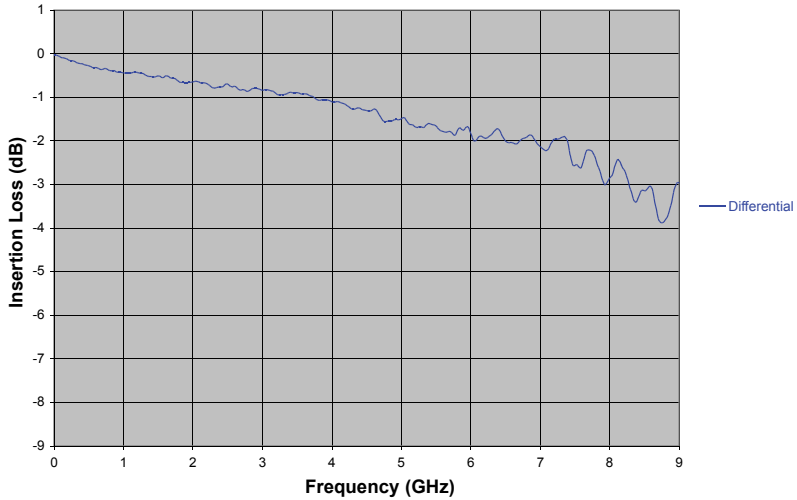
At time zero, the characteristic will be measured, or calculated, and a corresponding point will be made on the graph. At a later point in time, another sample is taken, which is again plotted on the graph. Sampling is repeated at defined intervals for the desired time period. A time domain plot essentially describes the behavior of a particular characteristic over a certain period of time.



Impedance plot in the time domain

Understanding Frequency Domain

In the frequency domain, the horizontal axis of a data plot represents the frequency of a constant amplitude, sinusoidal signal. The vertical axis again represents a particular characteristic of a component. At the first frequency, such as DC (0 Hz), the device is stimulated with a DC signal, and the particular characteristic of interest is measured or calculated. Its value is then plotted on the Y axis. The frequency of the stimulus signal is then increased, another measurement is made and plotted, and so on. Therefore, a frequency domain plot describes how a certain characteristic of a component will vary with changes in the frequency of the signal that drives it.



Insertion Loss plot in the frequency domain

What's the difference?

Frequency domain data is essentially composed of a series of time domain measurements or calculations, and a straightforward computational conversion between the two domains can be accomplished using the Fourier Transform. Thus, it is common to present data in both formats, so the end user can choose whichever is most appropriate or intuitive.

It is important to keep in mind that many terms and parameters commonly used in the SI world are actually just different ways of describing the same physical characteristics of a component. This is especially true of certain data which is commonly reported in both frequency and time domains.

How are measurements made?

Time domain measurements may be made with an oscilloscope. A typical time domain SI test for an interconnect is made using a Time Domain Reflectometer (TDR). A TDR is constructed around an oscilloscope and a pulse generator. The TDR injects an electrical pulse into the circuit under test, and measures the signal reflected back by the circuit.

TDT (Time Domain Transmission) measurements can also be made with most TDR instruments. In a TDT test, a pulse is injected into the circuit, and the pulse, which emerges from the far end of the circuit, is measured.

Frequency Domain measurements can be made with an oscilloscope and a sinusoidal signal generator. However, most frequency domain measurements are made today with an integrated test instrument called a Vector Network Analyzer, or VNA. The VNA consists of a tuned sinusoidal signal source and receiver set. The device under test is inserted between the ports of the VNA, and the source is swept across the frequency band of interest. Measurements of the reflected and transmitted signals are sampled at various points across the frequency band.

The "vector" description associated with a VNA designates that the instrument is capable of measuring phase information of the test signal. Phase data is critical for accurate translation between time and frequency domains, and can provide valuable insight into circuit behavior.

SINGLE-ENDED VERSUS DIFFERENTIAL SIGNALING

It is beyond the scope of this handbook to delve into the intricacies of various signaling schemes, but it is important to understand a few basic facts about single-ended and differential transmission. In many cases, differential signaling can provide better SI performance, so it is frequently used in high speed systems.

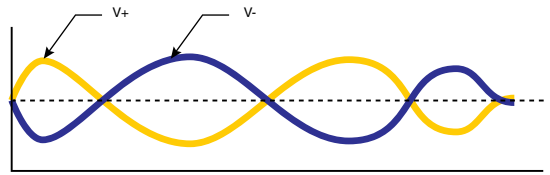
Single-Ended Signals

A single-ended signal is transmitted down a transmission line as a pulse referenced between a signal conductor and a return path. The return path is often referred to as "ground," but at higher frequencies the return path should be considered a critical part of the transmission line. The return path in a single-ended system might be a ground plane under a micro strip trace, an adjacent signal pin in a connector, or the outer shield of a coaxial cable. In a poorly designed system the return path might be unknown.

A single-ended signal is often visualized as a pulse whose amplitude switches between zero and a positive value, remains at the higher value for a certain period of time, and then returns to the zero level. For example, a single-ended voltage signal might switch from an initial state of zero Volts to a maximum positive state of +1 Volts. The signal will remain at +1 Volts for a certain period of time before returning to a level of 0 Volts.

Differential Signals

A differential signal consists of two separate pulses switching simultaneously. One signal will switch in a positive direction, say from 0 to +1 Volts, while its complement, or pair mate, switches in the opposite direction, in this case, from 0 to -1 Volts. If a differential signal is perfectly symmetrical or balanced, it will propagate effectively on two identical conductors. However, in many real world applications, a separate return path is used when practical, such as a shield in a twinax cable, since perfect signal symmetry is difficult to achieve and maintain.



Differential Signal Waveforms

Choosing connectors for optimal performance

Some interconnects are designed for optimal performance with differential signals, while others are optimized for best performance in single-ended applications. But that doesn't mean a "differential" connector won't work with single-ended signaling, or vice versa. In most cases, a lower speed rating can be expected when using an interconnect with non-optimal signaling schemes. Some interconnects are purposely designed to offer near identical performance for both single-ended and differential applications.

Many parameters critical to high speed interconnect performance will vary significantly depending upon the signaling scheme used. For example, the differential impedance of a certain connector will often be quite different than its single-ended impedance. For this reason, it is critical to use characterization data appropriate for the signaling scheme used in the system.

Core Parameters Impacting Signal Integrity

Many factors influence the suitability of an interconnect for high speed signal transmission. In this section, we discuss several critical electrical parameters in detail.

DETERMINING BANDWIDTH

To avoid costly over-design while ensuring system operability, any practical interconnect must have limits for the maximum and minimum frequencies of expected operation. Ideally, the bandwidth of the interconnect should be matched to the bandwidth of the system.

In some systems, the frequency bandwidth of concern is well defined, but in many applications, judgment is required. Such limits are often estimated by considering the fastest edge rate of the systems data signal. A rule of thumb is to divide 0.35 by the fastest signal edge rate. With this equation, a rise time in nanoseconds yields a bandwidth in GHz.

For example, a 1 nsec rise time has an associated frequency domain bandwidth of about 350 MHz (or 0.35 GHz). Similarly, a system with a 350 psec rise time has an estimated bandwidth of 1 GHz. A 35 psec rise time yields a 10 GHz bandwidth, and so on.

$$\frac{.35}{.35\ \text{nsec}} \approx 1\ \text{GHz}$$

Rise time to bandwidth equation

Although the mathematical justification is beyond the scope of this handbook, this rule of thumb is most accurate when rise time values determined by 10% to 90% measurements are used. That is, instead of using the amount of time it takes for a pulse to switch from the minimum "zero" level to the maximum "one" voltage level, the time is measured between the two points where the signal reaches 10% and 90% of its maximum level.

Common Rise Times	
Rise Time	**Bandwidth**
30ps	11.67 GHz
50ps	7 GHz
100ps	3.5 GHz
250ps	1.4 GHz
500ps	700 MHz
750ps	467 MHz
1 ns	350 MHz

INSERTION LOSS

Insertion Loss is the measure of total loss incurred by a signal as it travels through a component. The name is derived from the fact that, in effect, a reference test circuit is measured, then "cut" in half, and the device under test is inserted into it. The circuit is re-measured, and the resulting increase in loss is described as the insertion loss of the device under test.

The main factors that contribute to insertion loss are:

Reflection Loss - amount of signal energy lost due to impedance mismatches in the transmission line

Coupling Loss - amount of signal energy lost to crosstalk in other transmission lines

Dielectric Loss - amount of signal energy lost in the material dielectric

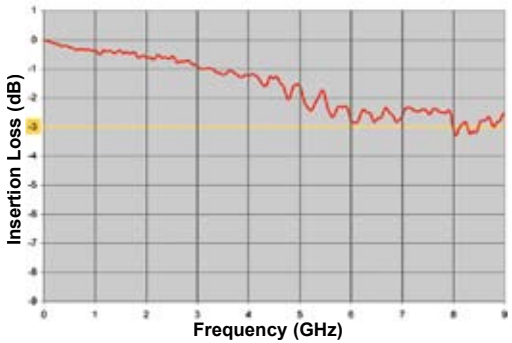
Conductor Loss - amount of signal energy lost in the signal conductors

Radiated Loss - amount of signal energy lost due to radiation

Keep in mind that these factors are inherent to the mechanical design of an interconnect. Little can be done by a system designer to change these factors after the interconnect has been designed and manufactured.

Significance of -3dB Insertion Loss

Typically the bandwidth of a component is determined by the -3dB insertion loss point. The -3dB point is defined as the frequency point where the signal is reduced to 70% of its original value. The significance of the -3dB point in communication circuits is supported mathematically by Shannon's Theorem.

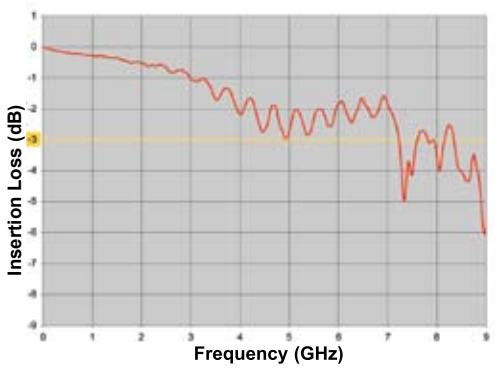


-3dB occurs at 8GHz

It must be emphasized that, although the -3dB rating may be a good approximation of a high speed connector, cable, or flex circuits performance, there are other factors that may be more critical to a particular systems ultimate performance.

Why "One Number" ratings can be counterintuitive

Insertion loss plots are not linear, so it is a good idea to evaluate data across the frequency band of interest, instead of relying on a single -3dB number. Occasionally when comparing -3dB points of similar connectors with different stack heights, the taller connector may appear to have a higher bandwidth rating. This is counterintuitive, as a taller connector will typically induce more loss and therefore have a lower bandwidth. A likely explanation is that the insertion loss experienced a resonance "valley" at some point on the curve. Because of conductor loss "tuning" effects, the resonance may have been more significant in the shorter stack height version than in the taller connector, so it would appear to have more loss at the resonant frequency. But typical loss values for the shorter connector will likely be lower than for the taller connector at frequencies above and below the resonant point.



-3dB occurs at 5GHz and 7.2GHz

A more conservative bandwidth rating approach is based not only on the -3dB number, but also considers resonances in the insertion loss plot. If a resonance occurs at a frequency lower than the typical -3dB point, then the frequency of that resonance is used to determine the components bandwidth.

Bandwidth (GHz) versus Data Throughput (Gbps)

Bandwidth is specified in the frequency domain, with units of Hz (typically GHz in modern systems). However, many data systems are specified by their maximum data throughput, which is typically in units of bits or bytes per second (such as Gbps). Unfortunately, though these two ratings are strongly related, there is no absolute way to convert between the two. The system data transfer rate is highly dependent upon the signaling scheme, and the possible use of signal conditioning and processing. It is also sometimes specified by multiple individual channels working in aggregate.

However, a conservative rule of thumb is to simply double the frequency domain bandwidth rating in Hz to obtain a maximum rate of data transfer. So, an interconnect with a bandwidth of 1 GHz could support a data transfer rate of 2 Gigabits per second (Gbps). This rule of thumb is based on the assumption

$$1\ \text{GHz} \times 2 \approx 2\ \text{Gbps}$$

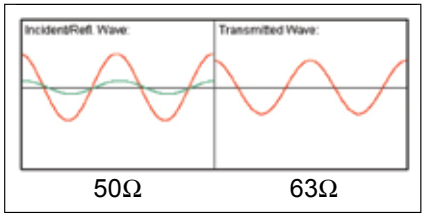
$$2\ \text{Gbps} \div 2 \not\approx 1\ \text{GHz}$$

Bandwidth to Rate of Data Transfer Rule of Thumb

of standard binary signaling. It does not account for potential data overhead requirements for higher level system functions such as error checking or routing. However, in the modern system environment, this number is still quite conservative. Data rates far in excess of twice the bandwidth can be achieved with advanced techniques such as signal conditioning, active noise reduction, and multi-level signaling.

IMPEDANCE

Signal reflections can be one of the biggest detriments to optimal system signal integrity. Reflections occur when a signal propagating down a transmission line encounters a change in the transmission path impedance level. Within an interconnect, these reflections result in signal loss and distortion. Reflections can also lead to increased crosstalk and EMC problems.



Reflections due to impedance mismatch

Impedance is defined as the cumulative reactance and resistance a circuit element presents to a circuit. It is often described as the level of opposition a component presents to an electric current.

An impedance discontinuity, or mismatch, occurs at every point in the transmission path where there is change in impedance the signal "sees." Reflections occur at impedance discontinuities regardless of whether the impedance discontinuity changes from a higher impedance to a lower one or vice versa.

When discussing impedance, two additional definitions are important: characteristic impedance and apparent impedance. Characteristic impedance is defined by physical parameters such as geometry (contact or cable design) and material properties (dielectric constant of the materials used in construction). The apparent impedance is dependant upon the signal's frequency content and the measurement or simulation environment.

If a signal path has a uniform geometry and construction then the characteristic impedance will be the same at any point along that path. Such a construction is called a controlled impedance line, the entire transmission line is defined by one impedance value. A non-uniform transmission line, such as a typical high speed connector, can have different characteristic impedance values along its length.

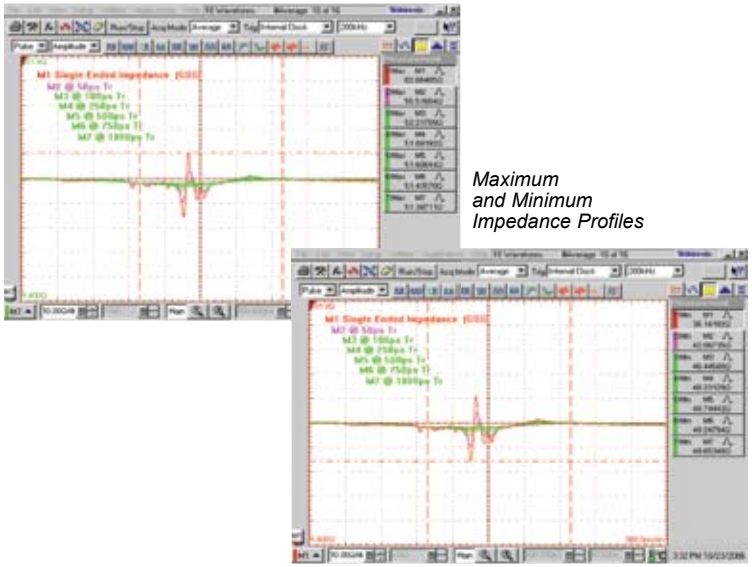
Why 50Ω or 100Ω Impedance

A TDR can be used to generate a plot of the impedance versus time of the interconnect path. Such a plot is referred to as an impedance profile. The actual physical distance along the circuit path can be mapped onto the impedance profile plot.

To determine absolute impedance values accurately, a TDR must reference its calculations to a transmission line of known impedance located between the pulse source and the device under test. Typically, a reference impedance level of 50 Ohms is used for single-ended measurements and 100 Ohms for differential measurements.

For SI applications, the minimum and maximum values presented in an impedance profile are usually of more concern than the characteristic impedance at various points along the plot. A rule of thumb when selecting an interconnect is to limit minimum or maximum impedance values to no more than 10% deviation from the system impedance level at the rise time or frequency band of interest.

A key point to note is that characterizing an interconnect in a 50 Ohm or 100 Ohm test environment does not imply that it is optimized for a 50 or 100 Ohm system. Such data only shows how the device performs with that particular reference impedance level.



Maximum and Minimum Impedance Profiles

Apparent Impedance

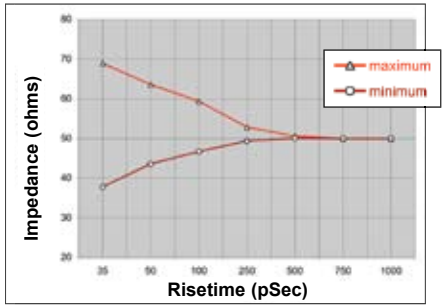
This brings us to the concept of apparent impedance. Apparent impedance is the effective impedance of a component when measured or used at a specific signal rise time or frequency, in a specific impedance environment. As rise times get slower and the frequency bandwidth goes lower, the effective, or apparent, impedance of a component moves closer to the impedance level of the circuit in which the component is being used.

At slow rise times the device will appear to have an impedance value close to the reference or system impedance. But as rise times decrease (in other words, as edge rates get faster) the measured impedance values begin to move toward the true characteristic impedance of the component. At an infinitely short rise time, we would measure the true characteristic impedance of a device.

This effect is important when seeking an interconnect solution for a system with an impedance other than that of the reference impedance used in the characterization process. In those instances, the impedance values at the fastest rise times on the TDR impedance profile should be used as an approximation of the interconnect's "true" characteristic impedance.

For instance, if a connector is desired for use in a 75 Ohm system environment, but the impedance profile was generated in a 50 Ohm reference environment, examine the impedance values at the fastest characterization rise times. Many typical high density connectors have a characteristic impedance greater than 50 Ohms. It is not unusual to find that the characteristic impedance of such a connector at a very fast rise time is actually about 70 Ohms. Such a connector will actually perform better in a 75 Ohm system than it would appear in the 50 Ohm test environment.

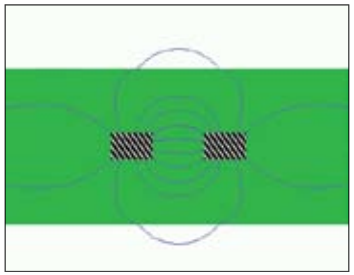
Again, the physical structure and material properties of a component determine the characteristic impedance, and signal rise time or bandwidth determines its apparent impedance. Physical parameters are evaluated and optimized in the early stages of a connector's design using electromagnetic modeling tools, and once tooled, cannot be changed. However, choice of signal-to-ground ratios and signal path assignments within an interconnect can result in configurations with significantly different impedances.



Impedance vs. Rise Time

CROSSTALK

Crosstalk is often a critical parameter to consider when selecting an interconnect for a high speed application. Crosstalk can be defined as noise arising from unwanted coupling of nearby signal lines. It occurs when two signals are partially superimposed on each other by inductive and capacitive coupling between the conductors carrying the signals. Crosstalk can result in distortion and degradation of the desired signals.



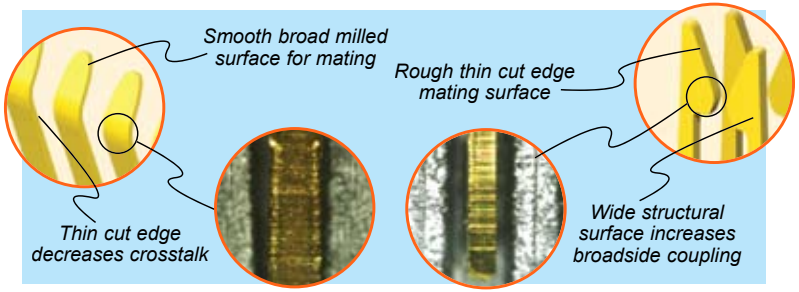
Field lines between two conductors

There are two types of crosstalk of concern in high speed systems, near end (NEXT) and far end crosstalk (FEXT). NEXT is the measure of the level of crosstalk at the transmitting end of the signal path, while FEXT is the measure of crosstalk at the receiving end of the signal path.

There are several ways to minimize crosstalk in a high speed interconnect:

Connector Contact Design

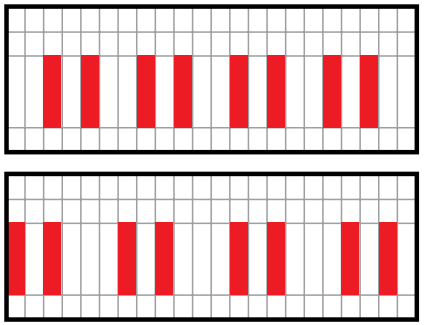
To reduce capacitance between victim and aggressor signals, it is often desirable to minimize the amount of broad-side coupling between connector contacts. This effect can be envisioned by considering a simple capacitor, which consists of two conductive plates separated by an insulating dielectric. By minimizing the amount of parallel metal surface area, capacitive coupling is reduced. This can be difficult to achieve with side-by-side stamped contacts, and as a result, is often addressed by using a formed contact design. That is, a design where the two "plates" are essentially placed flat in the same plane, so that direct coupling only occurs on the much smaller edge of the plates. Through field solver simulations, the SI performance of various contact designs can be evaluated and optimized before a contact is tooled.



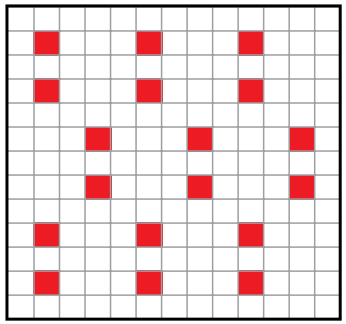
Formed contact vs. stamped contact

Contact Spacing

As the distance between contacts increases, inductive and capacitive coupling both decrease. This effect can be observed in an electromagnetic field plot by the reduced number and density of field lines connecting the two conductors. For example, a connector with terminals spaced on a 0.8 mm pitch will typically have better crosstalk performance than one with a 0.5 mm pitch. In differential pair systems increasing the distance between adjacent pairs minimizes coupling and, in some cases, eliminates the need for interstitial grounds, so total signal density can be increased.



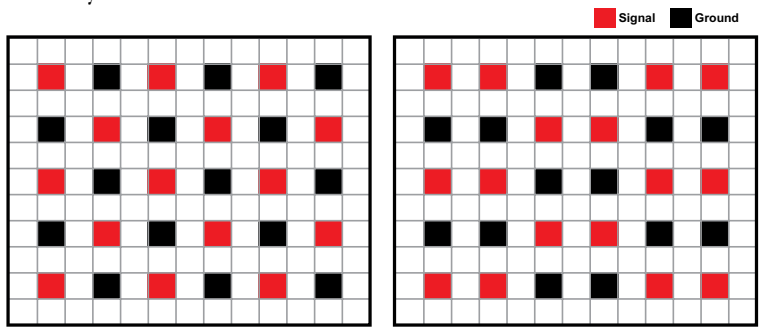
Separate with greater pitch spacing



Separate with interstitial spacing

Pin Mapping

By assigning pins between signals as return paths (grounds), unwanted coupling between signal pins can be minimized. For high speed applications a 1:1 signal to ground ratio is typically optimal. Pin mapping for SE applications would then be S-G-S-G, while DP applications would use DP-G-DP-G. These pin assignments provide a good performance versus density trade-off. Of course, more return paths could be added between signals to increase isolation for applications where crosstalk must be extremely low. However, this greatly reduces signal density of the interconnect.

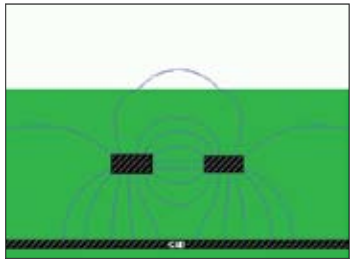


Single-Ended

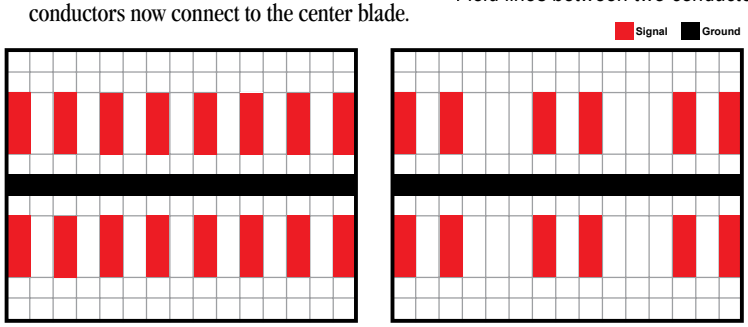
Differential Pair

Integral Ground Blades

By providing a return path through a center ground blade or plane, row to row crosstalk (across the blade) can be reduced to near zero. Coupling between pins within a row can also be reduced with such a plane. This effect can be observed in an electromagnetic field plot, where some of the field lines that would have connected to other signal conductors now connect to the center blade.



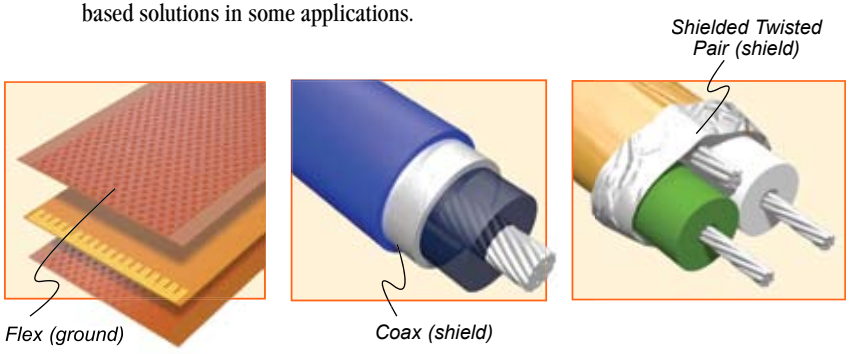
Field lines between two conductors



Single-Ended *Differential Pair*

Shielding

In high speed cable and flex circuits, shielding is sometimes used to minimize line to line coupling. Shielded coax, twinax, or twisted pair cable, combined with high speed connectors, provides optimal low crosstalk cable assembly solutions. High speed flex circuits use ground planes to the same effect. By locating the flex circuit ground plane very close to the signal lines, (typically much closer than in a connector), signal lines are coupled much more tightly to the ground plane than to other signal traces. As a result, crosstalk is reduced, and impedance can be controlled effectively. Such constructions allow high speed interconnect solutions based on flex assemblies to out perform cable based solutions in some applications.



High Speed Characterization Reports

Connector High Speed Characterization Reports provide time domain crosstalk data for various signal configurations, for both differential and single ended applications. Typical "best case" and "worst case" numbers are reported. Best case is usually measured with a ground pin located between each signal line or differential pair. For a typical worst case scenario, no grounds are used between the signals or differential pairs.

It should be noted that the pinouts used to define "worst case" and "best case" measurements can vary significantly between various types of connectors, such as two row connectors versus multi-row "array" type connectors. Such information should always be clearly detailed in the characterization report.

Crosstalk is calculated as a ratio of the measured input line voltage to the coupled line voltage. In most reports, measurements are a single disturber (aggressor) with the input line sometimes described as the "active" or "drive" line. The coupled line is sometimes described as the "quiet" or "victim" line. The crosstalk ratio is tabulated and reported as a percentage.

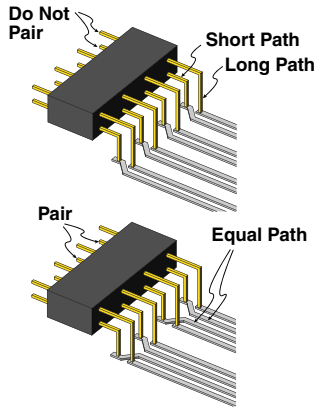
As a rule of thumb, 10% crosstalk levels are often used as a first pass limit for determining acceptable interconnect performance. However, system crosstalk tolerance can vary greatly. Some systems may require levels as low as 1%, while in others, crosstalk might be nearly irrelevant, and 30-40% levels may be perfectly acceptable.

PROPAGATION DELAY AND SKEW

Propagation Delay is defined as the amount of time it takes for a signal to propagate through an interconnect path. Knowing the propagation delay of the various signal paths can be critical for system timing analysis.

Skew is defined as the difference in propagation delay between two or more signal paths. Low skew between multiple paths can be important in a parallel bus. Of greater concern is the impact of skew between two conductors of a differential pair. If both path lengths aren't matched precisely, skew in a differential pair can lead to increased insertion loss, impedance mismatch, crosstalk and EMI.

Propagation delay and skew are related to the frequency domain property of insertion loss phase.

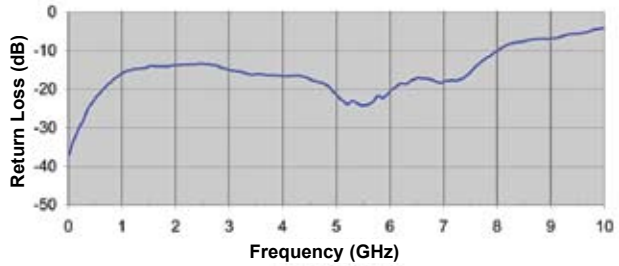


Other Common Signal Integrity Related Parameters

In addition to the core performance factors described previously, several other parameters are often encountered in the SI world. In general, most of these parameters are essentially derivatives of the core parameters. Changes in the core parameters will result in changes to the derivative parameters as well.

RETURN LOSS

Return Loss is a frequency domain parameter analogous to the time domain impedance profile. Return Loss is defined as the amount of signal energy reflected back towards the source as a result of impedance mismatches in the transmission path. As mentioned, there is little a system designer can do within a connector or cable assembly to affect impedance. The only variables affecting return loss which are under the system designer's control are system impedance matching, signal path assignments and the bandwidth or rise time of the transmitted signal.



Return Loss plot

As a rule of thumb, return loss values of less than -10dB in the frequency band of interest are desirable for many applications.

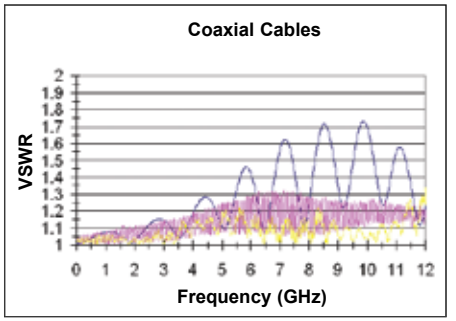
VOLTAGE STANDING WAVE RATIO

Another way of characterizing the effects of impedance mismatch in the frequency domain is Voltage Standing Wave Ratio (VSWR). VSWR describes the ratio between the steady state Voltage measured at either side of an impedance mismatch.

VSWR is commonly used in RF and microwave environments. It is often specified as a "one number rating," especially for coaxial connectors. In such cases, it is assumed that the impedance mismatch caused by the connector will be the dominant electrical characteristic limiting its performance in a high frequency system.

For example, performance data for a coaxial connector might simply be provided as "VSWR 1.20." This is shorthand for an implied maximum VSWR of 1:1.20 at the connector interface, when used in a system with an appropriate impedance, and across the frequency band of interest.

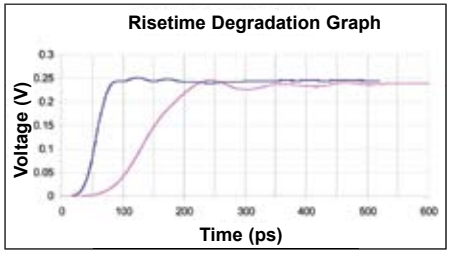
Since VSWR and Return Loss are both impedance related, they are directly proportional. VSWR can provide quick insight into the amount of power that is reflected back into a transmitter from an interconnect. Return loss provides similar insight into the eventual level of a signal that is transmitted through the same interconnect. Thus, both parameters can provide useful insight.



VSWR plot

RISE TIME DEGRADATION

Rise Time Degradation is a time domain description of the phenomenon where the rise time of a signal is slowed as it propagates through an interconnect path. Rise time degradation can become a significant problem when the rise time is slowed to near half the system bit rate. At that point, the receiver is no longer able to detect a change in logic state. In effect, the signal no longer has enough time to reach the logic one state before it begins switching back to a zero state.



Input of 37ps and Output of 116ps = 309% Rise Time Degradation

It should be noted that failure to account for the effects of rise time degradation in the system can lead to costly over-specification of system components. For example, a certain transceiver chip might be rated as delivering an output pulse with a 50 psec rise time at the package lead. But by the time the signal travels through several inches of PCB trace, rise time degradation might have slowed its rise time significantly. For instance, the rise time might actually be 150 psec

when the signal encounters its first connector. In such a case, the interconnect path from that point may be evaluated under the assumption of a 150 psec application versus the more stringent 50 psec assumptions.

ATTENUATION

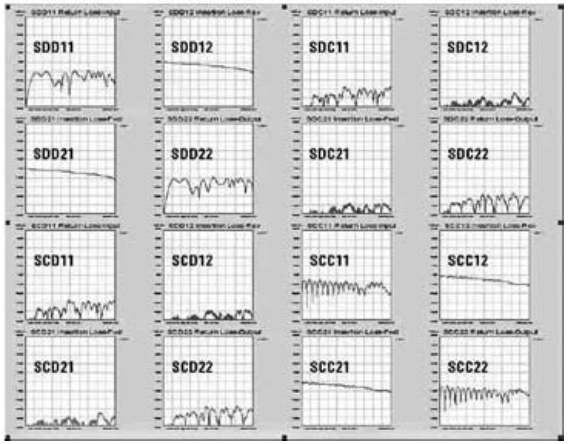
Attenuation is a frequency domain parameter, and is a term very closely associated with insertion loss. In fact, the two terms are often used interchangeably. There is not complete agreement within the industry as to the exact differences between the two terms, so care should be used in determining exactly how the term attenuation is used in a particular context.

Most commonly, attenuation is defined as all losses caused by a device except impedance mismatch losses. By this definition, if a device is used in a perfectly matched circuit, the insertion loss and the attenuation will indeed be equal.

S-PARAMETERS

S-parameters, also known as scattering parameters, are a unified set of frequency domain parameters that can be used to completely define the properties of an electrical device. S-parameters can be conveniently measured with a modern VNA. They also lend themselves well to rapid mathematical manipulation, and thus offer the potential for use in circuit simulations.

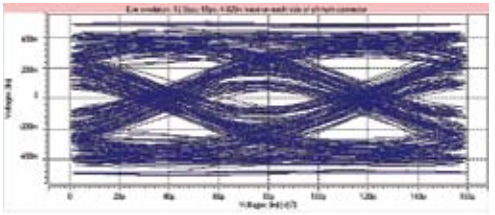
S-parameters can be defined for single port or multi port applications, and are therefore suitable for single-ended and differential applications. S-parameters can be mapped directly to parameters such as insertion loss (S21), return loss (S11), and crosstalk (S13, S14), so in theory, they can be used to fully characterize an interconnect path.



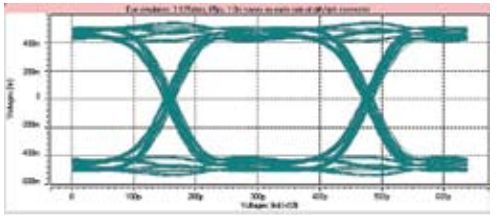
Multi port, mixed mode S-parameters

EYE PATTERNS

Eye patterns are a time domain characterization of system level performance. Eye patterns are generated by sending continuous streams of data from a transmitter to a receiver, and overlaying the received signals upon one another. Over time, the received data builds to resemble an eye. Negative SI effects in the transmission path can cause the signal to distort, which over time, will cause the eye to "close." Specifications, such as an eyemask template, can be placed on the amount of open area required in the eye to ensure a functional system.

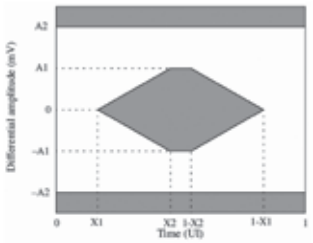


Closed "Eye"



Clear "Eye"

Eye pattern specifications may be placed on an entire interconnect path, that is, from a transmitter to a receiver. However, when used to evaluate a particular component of that path, say, a single connector, eye patterns fall short. While it is likely that a single component that fails to meet an eye pattern requirement will also cause an entire interconnect path to fail, the converse is not necessarily correct. In other words, a component (or all components in an interconnect path, for that matter) might pass an eye pattern test when tested separately, but a complete path containing that component might not pass the same test.



Eye mask template

Test circuit eye waveform with eye mask

SIGNAL INTEGRITY PRODUCTS AT SAMTEC

Samtec addresses Signal Integrity requirements in a variety of board-to-board, cable-to-board, and panel-to-board architectures spanning distances of 3mm to 3 meters and beyond. If signal density is a greater concern than absolute highest speeds, Samtec's SI segment also contains some of the highest density interconnects in the entire product line.

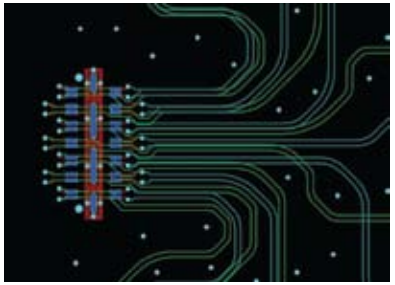
Samtec's SI products are designed for situations where the interconnect must have minimal impact on the transmitted signal. SI performance in connectors is maximized using means such as contact and housing design, material properties, pin spacing, ground planes and shields. Longer interconnect solutions utilize high speed connectors combined with riser cards, flex circuits, micro coax and twinax cables designed for low loss, minimal crosstalk and controlled impedance.

Please contact **SIG@samtec.com** for more information.

Importance of the PCB Break Out Region (BOR)

High speed performance of PCB mount connectors must be considered in the context of the application in a real world environment. "Connector-only" data can be useful for comparing the relative performance between two similar connectors, but it may be very far removed from the performance practically obtainable in an actual application.

This is mainly due to effects of the PCB traces and ground planes in the vicinity of the connector. This region is often referred to as the "break out region," or BOR, because in this area, traces are "broken out" from an optimized, consistent transmission line environment, and routed as required to attach to the connector terminals.



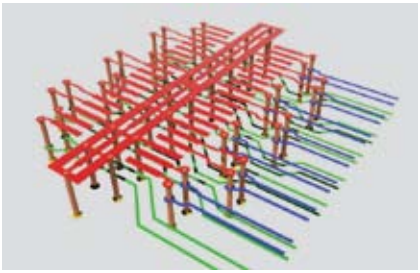
Break Out Region

In high speed applications, well referenced, controlled impedance traces are used to transfer signals from the transmitter IC to the first half of the separable connector. Similar traces also carry the signal away from the second half of the connector and across the second PCB to the receiver system. Depending on the application, these traces will be designed as either single-ended traces (typically 50 or 75 Ohms), or differential pairs (typically 100 Ohms).

Signal Trace Design

Single-ended traces are referenced to an adjacent ground layer. There are two approaches to differential trace design. Differential traces may be designed as stand alone, tightly coupled pair groups, or they may be designed as two single-ended traces. In this approach, the two traces are well referenced to an adjacent ground plane, but only weakly coupled together as pair mates.

To minimize crosstalk, it is almost always desirable to minimize coupling between signal conductors. Therefore, multiple single-ended traces are spread out as widely as possible. It is also desirable to couple differential pair mates as tightly as possible, while at the same time, separating each



3D Model of BOR

pair from other pairs to the greatest extent practical. When such an optimal trace design has been developed, the traces are typically fanned out from the transmitting IC into a pattern of constant cross section traces in the PCB.

To maximize density and enable manufacturability, PCB mount connectors are often designed with a terminal pitch and arrangement that may be quite different than those of the optimal PCB traces. In connectors designed for high speed applications, this pattern will most likely be designed for optimal high speed performance in the connector itself.

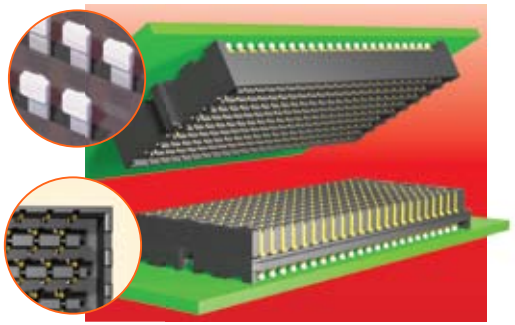
Transitioning the traces from the optimal PCB transmission line pitch and arrangement to the different connector pitch and arrangement can be problematic, even under the best of conditions. Physical space limitations in the area of the connector imposed by necessary signal vias, connector mounting holes and solder pads add to the challenge.

Therefore, great care must be taken in trading off PCB manufacturability requirements with desired Signal Integrity performance in the BOR near a high speed connector. In fact, signal degradation caused by BOR effects is often greater than that which is caused by the connector itself.

Optimizing the System rather than the components

In some recently developed high speed connectors, trade offs have actually been made in connector-only performance to allow easier and more optimal trace routing, which minimizes signal degradation in the BOR. In such cases, while the connector-only data may look less than optimal, a net gain can be achieved in the overall performance of the PCB/connector assembly.

Another factor to keep in mind is that ground planes in the PCB can interact electrically with the connector and its mounting pads. So the properties of a ground plane, and its location relative to the connector, can have a significant impact on the high speed characteristics of the PCB/connector assembly.



Differential Pair array provides optimized routing

Some connector vendors provide prospective customers with test PCBs optimized for the connector of interest. Such boards typically contain well controlled traces routed from the connector under test to coaxial test port connectors (typically SMA) on the board periphery. The test ports allow direct attachment to high frequency test instrumentation.

The system designer should be aware of the design philosophy used in designing the particular test boards being used. Some boards are optimized for minimal impact on the test signal. Such boards might be made of high performance board materials and use trace routing densities much less than would ever be considered in a real world application. The intent of such boards is to provide the user with results very similar to connector-only data.

Test boards might also include calibration or de-embedding structures. With proper techniques, such boards can allow the effects of the PCB and BOR to be removed from the measurement. These boards provide results close to connector-only performance. Such boards are most appropriate for use in extracting connector models from test measurements. However, the designer must keep in mind that such a level of performance might never be achievable in a practical, real world system design.

A better way to evaluate connector/system performance

By now, it should be clear that a designer expecting in-system performance on par with connector-only data may be in for an unpleasant surprise!

A more reasoned approach is to characterize the connector and the PCB as a complete system. Only in this situation can all interactions between the board and the connector be observed and characterized. Of course, this approach has its drawbacks too, as no two systems are exactly alike. So each system must be modeled and/or tested individually to completely characterize its performance. However, by carefully constraining the problem and accepting a few generalizations, a very practical and useful solution can be achieved.

While most interconnect systems are indeed unique when considered from end to end (transmitter to receiver), there is often much consistency in the BOR region design associated with a particular connector. This is due to the fact that the connector footprint is a constant, and the transmission line trace geometries are often quite similar in many designs.

Connector vendors can take advantage of this fact and offer optimized footprint and BOR reference designs for their connectors. Such designs will, out of necessity, be limited to certain board materials, thicknesses, stack ups, i.e., signal and ground layer assignments and connector signal mappings.

These designs will typically be optimized for maximum high speed performance. Ideally, the footprint design will provide guidelines for routing signal traces through the challenging area of the PCB located beneath the connector, thus saving the board designer much time and frustration.

SAMTEC FINAL INCH® PCB DESIGN TOOLS

Samtec takes the concept of providing BOR reference designs a bit further with its Final Inch® PCB design tools. Samtec's Final Inch® designs are engineered to offer the optimal trade offs between low cost, industry standard PCB materials and processes, and high speed signal integrity performance.

For ease of import into a variety of PCB layout packages, Samtec provides Gerber files of the PCB BOR design. To further aid the PCB designer, designs for 50 Ohm single-ended and, where appropriate, 100 Ohm differential transmission line traces are also provided.

To assist the system designer, Samtec also provides validated SPICE models of the entire interconnect path, including the mated connector pair, BOR and length scalable traces. These models can be downloaded and pasted into a simulation of the complete system.

Physical samples of PCBs based on the Final Inch® BOR designs are also provided by Samtec, free of charge. These boards are designed to interface to standard signal integrity test equipment, and include SMA connectors with a launch optimized for use to 20 GHz. These test boards provide an excellent test vehicle for determining real world performance of the trace/BOR/connector system.

Samtec goes even one step further and provides protocol specific Application Notes based on Final Inch® interconnect designs. The Application Notes are based on simulations using industry standard protocols such as PCI Express, RapidIO, XAUI, and Serial ATA (SATA). The simulations use models of commercially available transceiver sets, under worst case conditions. Trace lengths are varied until received eye patterns no longer meet specifications. Application notes add yet another level of confidence that a Final Inch® based system design will be right the first time.

Please visit **www.finalinch.com** for additional information.

Electromagnetic Compatibility

Electromagnetic Compatibility (EMC) is a topic closely related to SI. EMC is achieved when an active electronic device is capable of operating without emitting electrical noise that could disrupt other electronic devices which may be operating nearby. Such noise is called Electromagnetic Interference (EMI).

Almost any active AC electronic or electrical circuit is capable of generating noise, but generally, the higher the frequency of operation, the more likely the device is to cause EMI. Similarly, an active device must be capable of operating properly in a moderately noisy environment. This is often referred to as being immune from EMI.

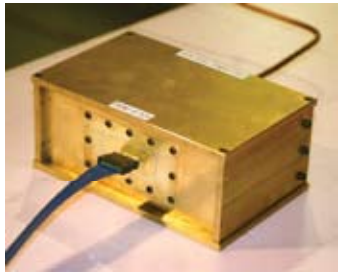
EMI can be radiated or conducted away from or into an electronic device. Connectors and cable assemblies can contribute to EMC issues by radiating or coupling energy from noise sources. Signals that have periodic switching such as clocks are a classic noise source. If energy from this type of source couples to a cable that exits a shielded enclosure, the cable can radiate the coupled noise much like a cell phone antenna radiates (although not as efficiently). Placing a shield over the cable (and terminating the shield properly) can reduce the radiated emissions dramatically. For a board-to-board connector inside an enclosure the situation is similar, with the exception of the radiated emission occurring inside the enclosure, thus the radiated emission may or may not be visible during an EMI test.

EMI Shielding Test Chamber

Because of the serious nature of EMC issues, many governments require EMI compliance testing of active electronic systems. For example, in the US, such regulations are administered by the Federal Communications Commission (FCC). Militaries also require compliance testing, and these requirements are normally more severe than typical government requirements. Some governments also require susceptibility testing to ensure a device is immune to typical levels of EMI.

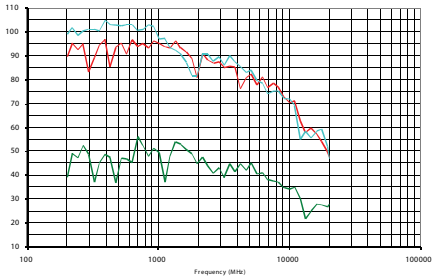
While passive components can impact the overall system level EMC performance, it is not possible to directly test a connector, cable assembly, resistor or bolt for EMI compliance.

EMI compliance is typically performed at the end of the product development cycle when few design options exist if a product fails the test. Since the cables might be radiating, changes to the cable can improve performance. Minor EMI fixes include filtering, shielding improvements and chassis shielding improvements. Major EMI fixes include PCB redesign to increase the isolation of noise sources. Unfortunately, some industry standard interfaces (USB, Firewire, Ethernet, Infiniband, etc.) may or may not have EMI problems depending on the implementation.



EMI Compliance Testing

While cables and connectors cannot be tested for compliance, their shielding performance can be tested or simulated. EN61000-4-21 Annex F is a test method developed to determine shielding performance, and other techniques exist to measure transfer impedance, screening attenuation, common mode power transfer, etc. Each of these terms has a specific definition and is used in reference to a specific test methodology.



Shielding Effectiveness Plot

Meaningful shielding tests must mimic the installation/application and this complicates the test fixture. Because of these challenges, the connector/cable industry has largely avoided providing shielding information on high density, multi-pin products.

Samtec has performed comparison testing on typical board-to-board connectors with and without shields. Testing showed an improvement of 10-20 dB over the frequency range of 1-4 GHz and 0-10 dB from 4-10 GHz. Full wave simulation showed an improvement of approximately 10 dB over the 1-10 GHz frequency range as well.

Shield Comparison Testing

Design practices that are good for SI are nearly always good for EMI. One practice is to allocate ground pins in high density connectors and sockets to serve as the return path for high speed signals. This practice reduces crosstalk and improves the impedance control through the connector. It also reduces the voltage potential developed across the connector (ground bounce) which can act as an EMI noise source. Differential signaling can significantly reduce crosstalk which helps with SI, and it reduces common mode noise developed across connectors, which is good for EMI.

Encoding and signaling choices can have a dramatic impact on EMI performance and may or may not impact SI. A technique called spread spectrum clocking (SSC) is used on several interface standards such as PCIe, SATA and SAS. This technique adds a small, controlled amount of jitter to the clock signal and can reduce radiated emissions by 10+ dB. This approach reduces timing margin as it adds jitter, so it is not necessarily good for SI. Pre-emphasis is a wave shaping technique that distorts the transmitted signal in a controlled manner so that the effects of attenuation in cables or backplane traces are compensated for and implemented for SI purposes. This technique increases the high frequency content in the system, which is never good for EMI, so this is another example where SI and EMI design approaches are in conflict.

In summary, EMI and SI design strategies at the hardware level (connectors, cables and PCBs) tend to be complimentary. The mitigation approaches at the architecture levels (encoding scheme) are typically more independent and in some cases in conflict.

Interconnect Modeling

During a system's design phase, obtaining an assessment of signal integrity performance of the design may be required before moving onto the development of a physical prototype. To support this system-level assessment, a design team needs electrical simulation models of the devices specified in their design. Obtaining interconnect models that support the type of signal integrity analysis required can be a daunting task. The following information is intended to assist in understanding what to look for when requesting models from connector vendors.

Before beginning a search for connector models, it is suggested to consider the following:

Who are the manufacturers and what are the specific part numbers of the connector system?

Typically, interconnects used to connect two subassemblies involve a separable interface based on two individual components. For example, a connector system that connects two PCBs involves two individual connectors, commonly referred to as "terminal" and "socket." Electrical simulation models of connectors will represent a MATED pair of connectors.

If the separable interface employs the use of an edge card connector, the connector model should include the PCB connector mated with the edge finger pad that is recommended for the connector.

Some designs employ a non-separable interface, such as a board stacking pin header, or other one-piece interface connector systems. In that case, the connector model would be for just this one part.

What signal integrity parameters need to be simulated?

The signal integrity parameters one wishes to analyze will determine the type of model structure required. Connector models are available in the following structures:

- **Single-Line:** The single-line structure is used to evaluate the effects of a single set of connector pins. Typically, most single-line models represent a fully referenced pin (neighboring pins assigned to ground return).
- **Multi-Line:** This structure couples, in three dimensions, all pins to one another. This results in a complex model of an array of pins which include pin-to-pin coupling effects. Multi-coupled line structures offer the user the ability to choose different signal-to-ground (S/G) ratios and analyze for coupled noise, at the price of longer simulation run time.

The following table presents an overview of the signal integrity parameters that each structure can support:

ANALYSIS	Single-Line (1)	Multi-Line (2)
Characteristic Impedance (low-loss approximation)	yes	yes
Propagation Delay	yes	yes
Crosstalk	no	yes
Eye Diagram	yes	yes
Insertion Loss	yes	yes
Return Loss	yes	yes

(1) Only for a single aggressor within the model's defined signal-to-ground ratio
(2) For multi-aggressors within any signal-to-ground ratio allowed by the model's array size

Connector model limitations

An important caveat to consider is that, although the model structure can support the analysis of a specific signal integrity parameter, the accuracy of an analysis will be dependent on the complexity and quality of the connector model. To better understand the limitations of a specific connector model, the following must be understood:

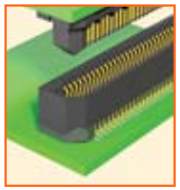
What are the defined "boundaries" of the connector model?

One way to categorize the boundaries of a connector model is as follows:

- **Boundary 1** - Connector components as a mated pair:
  - Model represents connector-only
  - Any part of the connector used for permanent PCB connection would NOT be included
  - For edge card style connectors, the recommended edge card pad would be included

1

- **Boundary 2** - Mated connector + permanent PCB connection
  - Pad area or via hole size specified per manufacturer's recommended PCB footprint
  - No footprint breakout trace routing included



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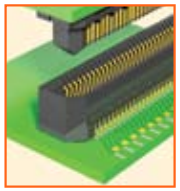
- **Boundary 3** - Mated connector + permanent PCB connection + breakout trace routing
  - Pad area or via hole size specified per manufacturer's recommended PCB footprint
  - Trace routing included for the break out region (BOR) of the connector, based on a pre-defined PCB stackup



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Typically, connector models offered within the industry fall into the "Boundary 1" category. Some vendors provide models for the other boundary definitions upon request (e.g., Samtec offers Final Inch® models for select connector series - visit www.finalinch.com for more information).

Was the model developed from calculations or from measurement?

Typically, models developed from calculations are derived from 2D or 3D field solvers. This technique allows flexibility when creating multi-line structures of several connectors within a specific product series (e.g., multiple board-to-board stack height combinations within a connector family).

The "quality" of the model generated from calculations is dependent on:

- The design of the connector pin field (e.g., open pin field vs. dedicated ground return contacts).
- The accuracy of the connector's CAD representation.
- Material properties included in the field solution and the accuracy of those parameters. For example, if the model does not include the dielectric loss properties of the housing, it will not be able to predict the dielectric loss component of the insertion loss.
- Defined maximum bandwidth of the model. In other words, the fastest signal rise time that can be applied to the model for a time-domain simulation or the maximum frequency that the model can support in a frequency-domain simulation.

Models developed from measurement are derived from empirical measurements of a connector within a defined test fixture. The effects of the test fixture are sometimes mathematically removed from the measurement, resulting in a model of only the connector.

This technique can provide models which include all of the physical properties of the connector. However, the models will have pre-defined pin mappings, and the more ports required, the more complex it becomes to develop a model from measurement.

The "quality" of the model generated from measurement is dependent on:

- The type of test instrumentation.
- The design of the defined test fixture.
- The accuracy of removing (de-embedding) the effects of the defined test fixture and the test instrumentation.
- Defined maximum bandwidth of the model. In other words, the fastest signal rise time that can be applied to the model for a time-domain simulation or the maximum frequency that the model can support in a frequency-domain simulation.

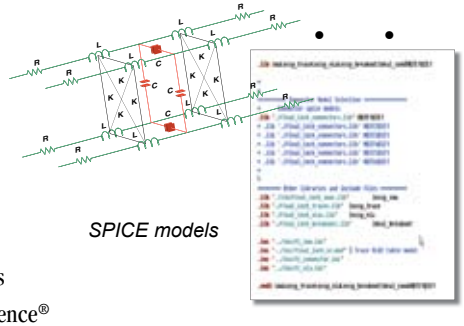
What is the simulation tool being used?

The answer to this question determines the required model format, or "syntax." The EDA (Electrical Design Automation) simulation "world" seems to divide models into two general format categories: SPICE and IBIS. This may be relevant for devices like ICs, but when it comes to connector models, this simple categorization falls apart.

SPICE models of connectors have been around for years, and certain defacto practices and standards have evolved. However, IBIS interconnect models are much less mature and continue to evolve. One issue to keep in mind with IBIS models is that the standard IBIS specification does not directly support connector models. Instead the IBIS ICM specification defines the connector model formats (reference http://www.vhdl.org/pub/ibis/icm_ver1.0/). So, unless the simulation tool supports models based on Berkeley SPICE or the IBIS ICM specification, connector models in the simulation tool's native format will be required.

This is an area where Samtec has taken the initiative within the connector industry, providing connector models for use in simulation tools other than SPICE. Samtec works with users to provide connector models for use in the following well-known EDA tools:

- Advanced Design System (ADS) from Agilent
- Allegro® PCB SI from Cadence®
- HyperLynx from Mentor Graphics
- HSPICE® from Synopsys
- ICX® from Mentor Graphics
- OrCAD® Capture from Cadence®



SPICE models

It is possible that the connector manufacturer cannot provide the required model for the EDA tool being used. It is also possible that the EDA tool cannot adequately analyze the required signal integrity performance parameters. In either case, the connector manufacturer may be able to provide additional signal integrity support in order to provide a performance assessment of their product within your design. Should you require such support on a Samtec connector, please contact the Samtec Signal Integrity Group – **SIG@samtec.com**.

Model Validation

Several methods are used to validate the accuracy and usability of circuit models. Currently, there are no industry standard procedures for model validation, formatting or functionality. Each component supplier must therefore determine their own acceptable levels of model accuracy, formatting and fitness for use. Ultimately, the system designer must determine if a supplier's models are "good enough" for use in a given situation.

In a typical validation effort, the accuracy of the model development process itself is first evaluated. Results from simulations with a typical model are compared against lab measurements of an actual component. Impedance, propagation delay, near end crosstalk, far end crosstalk and insertion loss are the key parameters evaluated.

Correlation of 10-15% in the specified model bandwidth is expected for most parameters. Because of the large dynamic range associated with crosstalk measurement and simulation, crosstalk is often over-predicted. Thus, it should be noted that models often present a worst case scenario in applications where crosstalk is an issue.

Slight tweaks to the model might be required at this step in order to increase accuracy. Impedance and propagation delay are typically considered to be the most critical parameters of the model. So accuracy in other parameters such as crosstalk might be traded in favor of increased accuracy in impedance and propagation delay simulations.

Models are also tested for ease of import and functionality by loading them into the relevant simulation tool and performing a basic test circuit simulation. For example, the optimal formatting for a model intended to be used in HSPICE will often be different than a model intended for use in a PSPICE simulation. Such differences might be as simple as acceptable nomenclature, naming conventions, or optimal sub-circuit nesting structure. Or in some cases, some types of models are specific to a certain brand of circuit simulator, such as the W-element in HSPICE.

In such cases, a component vendor might offer a "generic" model, and leave it to the system engineer to adapt the model to his particular circuit simulation tool. However, some vendors provide models in multiple formats, with each model already optimized for use in a particular simulation tool. In this case, it is important that each model be tested for functionality and ease of use in the particular simulation tool for which it is intended.

Additional Signal Integrity Resources

Samtec offers a variety of Signal Integrity support, services and resources via its online Signal Integrity Center:

- Signal Integrity Center: **www.samtec.com/signal_integrity**
- Signal Integrity Group: **SIG@Samtec.com**
- For more information about Final Inch® PCB design tools: **www.finalinch.com** or e-mail: **FI@samtec.com**
- For a list of current Samtec White Papers, Presentations, Articles and Press Releases: **www.samtec.com/reference/articles/white_papers.asp**
- For a list of upcoming and archived Samtec webinars featuring discussions on a variety of Signal Integrity and other interconnect-related topics: **www.connectorwizard.com/Webinars.aspx**

For additional Signal Integrity resources and training, Samtec recommends the following companies and materials:

- Teraspeed Consulting Group LLC provides assistance in the design and implementation of extreme performance systems: **www.teraspeed.com**
- Bogatin Enterprises, signal integrity specialists and a source for on-line training for world-wide engineers: **www.bethesignal.com**
- *Signal Integrity Simplified* (Publisher: Prentice Hall PTR; 1st edition (September 15, 2003)), by Eric Bogatin, is suitable for non-specialists, and offers a comprehensive, easy-to-follow look at how physical interconnects affect electrical performance.

An "open-mike" email reflector (currently administered by Ray Anderson at Xilinx) dealing with high-speed digital design issues is accessible via the following links:

- To administer your membership from a web page: **www.freelists.org/webpage/si-list**
- For help (include "help" in the subject field): **si-list-request@freelists.org**
- List technical documents: **www.si-list.net**
- List archives: **www.freelists.org/archives/si-list**
- Remote archives: **groups.yahoo.com/group/si-list/messages**
- Old (prior to June 6, 2001) list archives: **www.qsl.net/wb6tpu**

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